Dragonchip

Software Development Notice for DC6288F

AppNote300

Document Revision 1.1

November, 2019

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1 Introduction

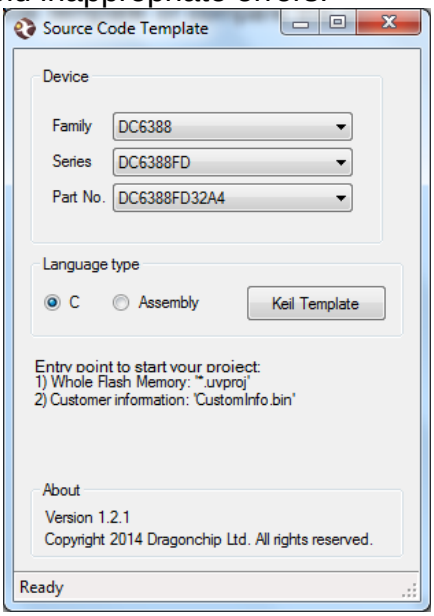
The Objective of this document is to show the important software development notice for DC6288F family. It is recommended to read this document before developing the MCU software.

2 Dragonchip Tools

2.1 Troubleshoot

Before software development, it is advised to review the AppNote303.

To start with software development, user can make use of the software 'Source Code Template' to create a template, in which all the necessary settings are made to avoid inappropriate errors.



In addition, the following should pay attention:

1. Avoid using generic pointer
   It was found the Keil C51's Generic Pointer implementation might not be supported by our MCU. Instead, memory-specific pointer is recommended, which fix its referencing memory space during variable declaration [1].
   An example is shown below.

Memory-specific Pointers

```
char idata * input_string; // memory pointer to indirect SRAM space
unsigned int xdata * cur_index; // memory pointer to XRAM space
char code * message; // memory pointer to CODE space
```

Generic Pointers *(Not recommended)*

```
char * buffer; // memory pointer that can points to SRAM, XRAM or CODE space
```

3 DC6288FD

3.1 Troubleshoot

	Topic	Symptom	Solution
1	Data flash memory initialization	Incorrect data flash content	1) If the Data Flash memory is initialized in the beginning of MCU software, add a 100ms delay before this initialization. Due to the unstable power supply at the moment of device power on, it is possible that Data Flash writing is failed. This 100ms delay at the beginning of the software help to delay the Data Flash writing before the power supply is stable. 2) Avoid initializing Data Flash memory by MCU software. It is recommended to download the Data File image to Data Flash memory by SLP.
2	SRAM initialization	Incorrect operation	The SRAM contents are undetermined in power up. That means the SRAM content can be any value. Please make sure the SRAM is initialized.
3	Data Flash memory access	1) CPU running suspended 2) Incorrect interrupt	During Data Flash access, CPU running is suspended while peripherals such as timers would keep running. 1) Do not assign any task until Data Flash access finished. Note that MCU could be reset by basic timer (watchdog) during Data Flash access. 2) Avoid interrupts during Data Flash memory access: ■ Only the first interrupt is processed even there are more than one interrupt during Data Flash access. ■ All interrupt will be delayed to be processed until completion of accessing Data Flash.
4	I/O port configuration in stop mode	High or unstable stop mode current	To prevent current leakage and minimize the stop mode current consumption, all the I/O ports should be correctly configured. The following configurations lead to “floating” state which are NOT allowed: 1) Input mode without pull up 2) Output mode, n-channel open drain, drive low, with pull up

			3) Output mode, n-channel open drain, drive high, without pull up 4) Output mode, push pull, drive low, with pull-up Hidden I/O pads which require above configuration handling.[1]
5	UART Data Transmission	Wrong UART data sent	Do not change the UART Transmit port (TXD) state when data is being sent out. Otherwise, wrong UART data may be sent.
6	Programming pins	Programming error	RSTN pin is reserved for multi-chip system to assert low to reset our CPU in order for synchronization. In case of single-chip system, the pin does not need to connect external reset circuit.[2] as internal pull-up is built-in. SL pin should not be driven by external circuit with the following: 1) Push-pull 2) Open-drain low 3) Loading cap In addition, if pull-up resistor is required in the circuit, it must be 100k ohm or higher. If pull-down resistor is required in the circuit, it must be 100k ohm or higher
7	Power Up I/O state	Undetermined	During oscillator stabilization wait time, all I/O are Hi-Z state except PB1 configuring with input pull-up.
8	Register 'FAM' bit 3	Undetermined	Chip with emulator function(JTAG pins) is prohibited to set bit 3 of register 'FAM' to 1

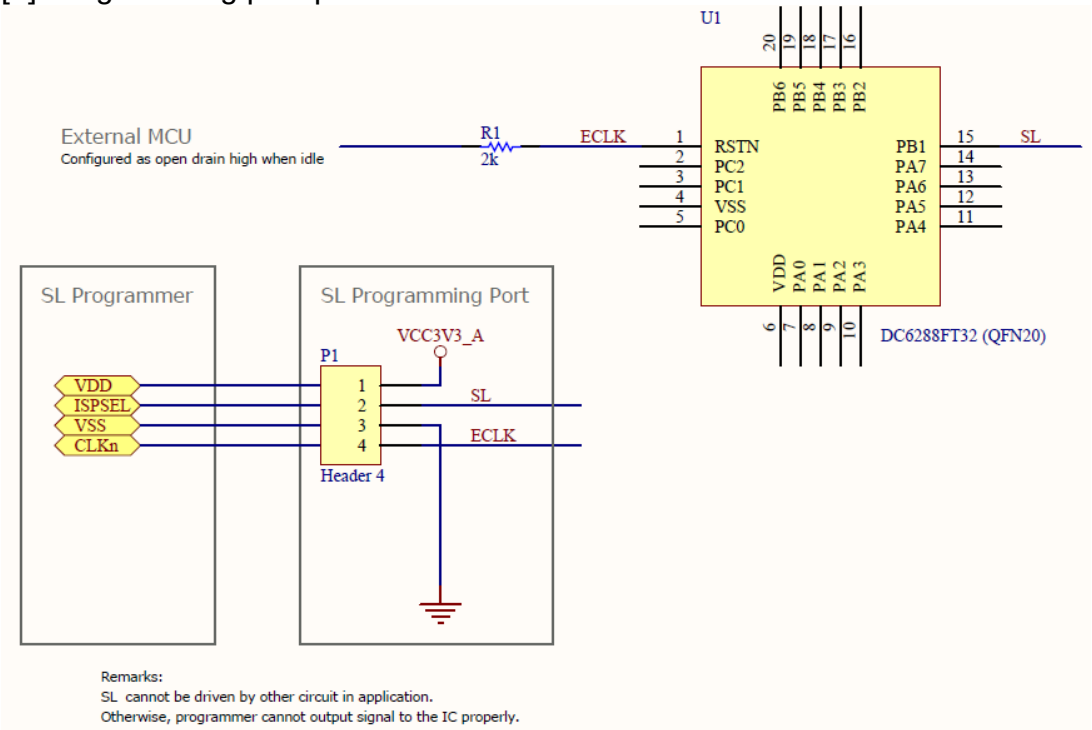
Remarks:
[1] Un-bonded I/O port (orange) is shown below. It should not be configured as "floating".

TSSOP-M	TSSOP-R	QFN20	QFN24	Pin Name
-	6	-	2	PC3
5	7	2	3	PC2
6	8	3	4	PC1
8	1	5	6	PC0
10	-	7	8	PA0
11	11	8	9	PA1
12	12	9	10	PA2
13	13	10	11	PA3
14	14	11	12	PA4
15	15	12	13	PA5
16	16	13	15	PA6
17	17	14	16	PA7
-	-	-	14	PC4
-	18	-	17	PB0
18	19	15	18	PB1
19	20	16	19	PB2
20	2	17	20	PB3

TSSOP-M	TSSOP-R	QFN20	QFN24	Pin Name
1	3	18	21	PB4
2	4	19	22	PB5
3	-	20	23	PB6
-	-	-	24	PB7

It is suggested that at the beginning of the program, the un-used / un-bonded I/O should be configured as either:
1 Input with pull up, or
2 Output push-pull

[2] Programming pins precaution

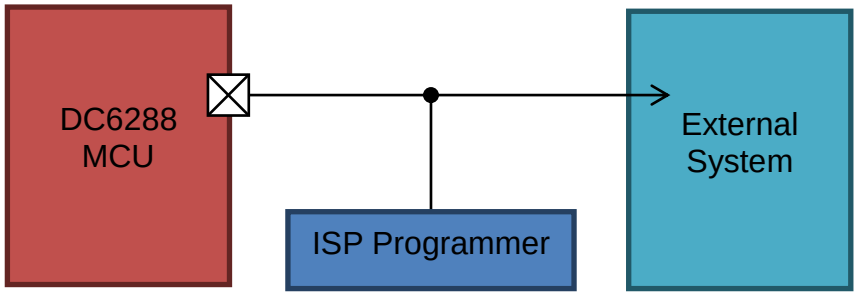


3.2 Hardware

3.2.1 Programming pins

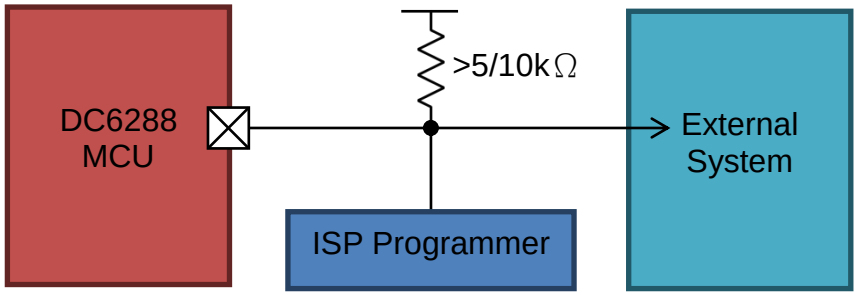
Precaution should be taken for the following I/O pins since they are shared with programming pins:
1 PB1

In order to do in-system-programming properly, below is a recommendation:
1 Push-pull output only
If the multiplexed IO is a push-pull output to external system's input, no additional isolation is needed.



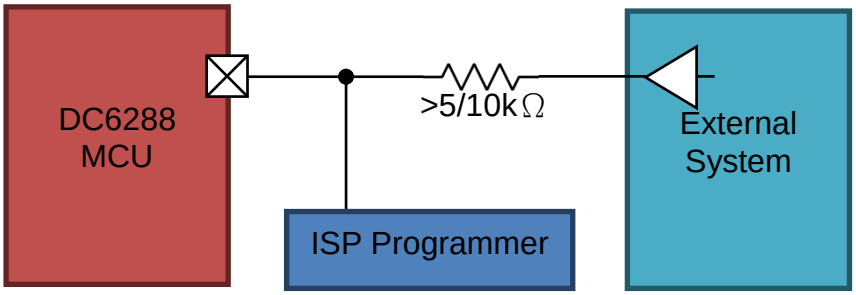
2 Open-drain output only w/ pull-up resistor

If the multiplexed IO is an open-drain output to external system's input with pulling resistor, the pulling resistors must not be under 5k Ohm for ISP of 1 to 2 devices and must not be under 10k Ohm for ISP of 3 or more devices together.



3 Input only or Bi-direction

If the multiplexed IO is an input to external system's output, an isolation resistor should be added to block the external system's driving affect the programming signal. The isolation resistors must not be under 5k Ohm for ISP of 1 to 2 devices and must not be under 10k Ohm for ISP of 3 or more devices together.

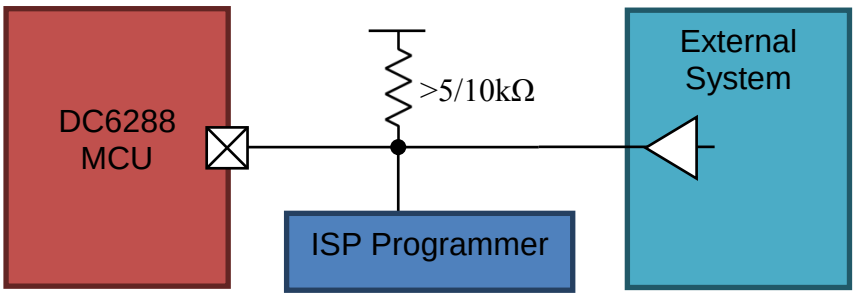


4 Input only or Bi-direction w/ pull-up resistor

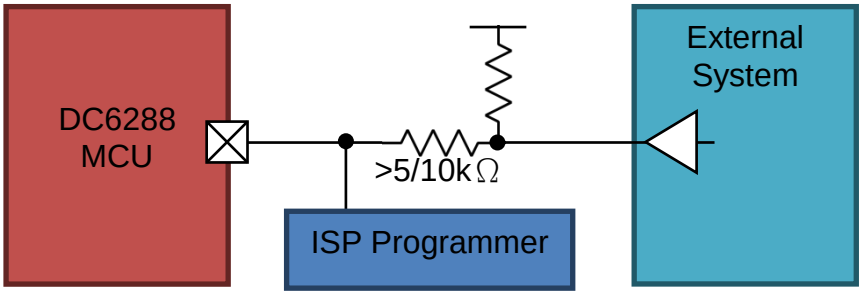
If the multiplexed IO is an input to external system's output with pulling resistor, the pulling resistors must not be under 5k Ohm for ISP of 1 to 2 devices and must not be under 10k Ohm for ISP of 3 or more devices together.

If the external system will not drain the signal line during ISP, no additional isolation resistor is needed. (Case 1) On the other hand, if the signal line may be drained by the external system during ISP, an isolation resistor should be added as shown below with resistance value over 5k Ohm for ISP of 1 to 2 devices or over 10k Ohm for ISP of 3 or more devices

together. (Case 2)



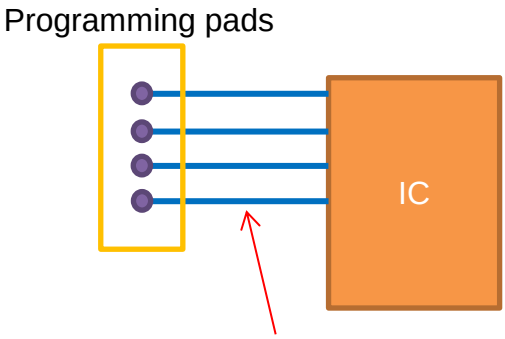
Case 1: External system will not drain during ISP



Case 2: External system might drain during ISP

3.2.2 PCB layout

Below are some guidelines for the layout.



No carbon film between pin and pad, and length < 3cm

3.3 Emulator Limitations

The emulator part number is DC6288EMT-FT (DCT-EDP (main unit)), download the latest user manual and refer to the limitation section.

3.4 In-System Programming

During programming, the flash memory has the following steps involved:

1. whole flash memory erase for security reason
2. write program flash memory
3. write customer information(Model/Version/Checksum)
4. read back program flash memory and customer information, and then verify byte by byte
5. lock program flash if required

3.5 Production highlights in customer factory

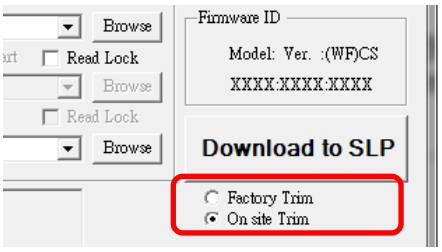
It is recommended to review the following items before production in customer site:

1 The prevention and control of Electrostatic Discharge (ESD)

2 PCBA level programming/trimming

2.1 Programming must be done at room temperature (25°C). It is advised to arrange 1 hour cooling between soldering reflow and programming/trimming on PCBA level

2.2 To obtain the best trimming performance, taking into consideration of PCB factor, it is recommended to do programming/trimming on PCBA level



And firmware is required to load ‘on site trim’ value at the beginning. Detail is available in source code template.

```
107  //--------------------------------------
108  // Main Program
109  //--------------------------------------
110  void main (void)
111  {
112  #ifdef FREQ_12MHZ
113    RCFREQ  = 0x00; // initialize the CPU running fre
114                    // before initialization, default is 4M
115    // for triming purpose
116    if ( (TRIM_V1 != 0xFF) && (TRIM_V2 != 0xFF) )
117    {
118      RCTRIM = TRIM_V1;
119      VREG2 = TRIM_V2;
120    }
121
```

Load ‘on site trim’

2.3 Trimming will be completed during programming stage

3 Routine check VDD from programmer to IC below 3.8V

4 Use SLP Programmer (DC6688SLP-USB Rev3.2 or higher)

5 Use Software SLP Rev6.9.3 or higher

6 The IC should be powered by our programmer ONLY

6.1 The programmer control power off/on to ensure proper programming & verification operations.

Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	Jun, 2018	All		First Release	Danny Ho	Patrick Li
1.1	Dec, 2018	3.2		Add section	Danny Ho	Patrick Li
		2.1		Add item for FAM bit 3	Danny Ho	Patrick Li

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