Dragonchip

DC6688F2SCN Application Note 051

System migration from DC6688F05S to DC6688F2SCN

Revision 1.0

Jan, 2009

Revision History

The following table shows the revision history for this document.

Date	Revision	Revision	Edited By	Reviewed By
Jan, 2009	1.0	Preliminary	Ken Yeung	Danny Ho

Contents

1 Introduction

The Objective of this document is to provide the DC6688F05S user on how to migrate to DC6688F2SCN.

2 Notes on firmware migration

Item		Description
A	Timer 0 and Timer 1 setting	the following condition at the same time happened is invalid: i) Timer 1 set to mode 1, and ii) Timer 0 set to mode 2

3 Further Notes on Firmware

This section applies to DC6688F05S/DC6688F2SCN.

Item	Description
a	Add 100ms delay at the beginning of the program
b	Initialization for SRAM
c	Counter A should be reset after exit from stop mode

For item a, add this delay at the beginning of the program to let the power stable before starting to run the firmware in production line.

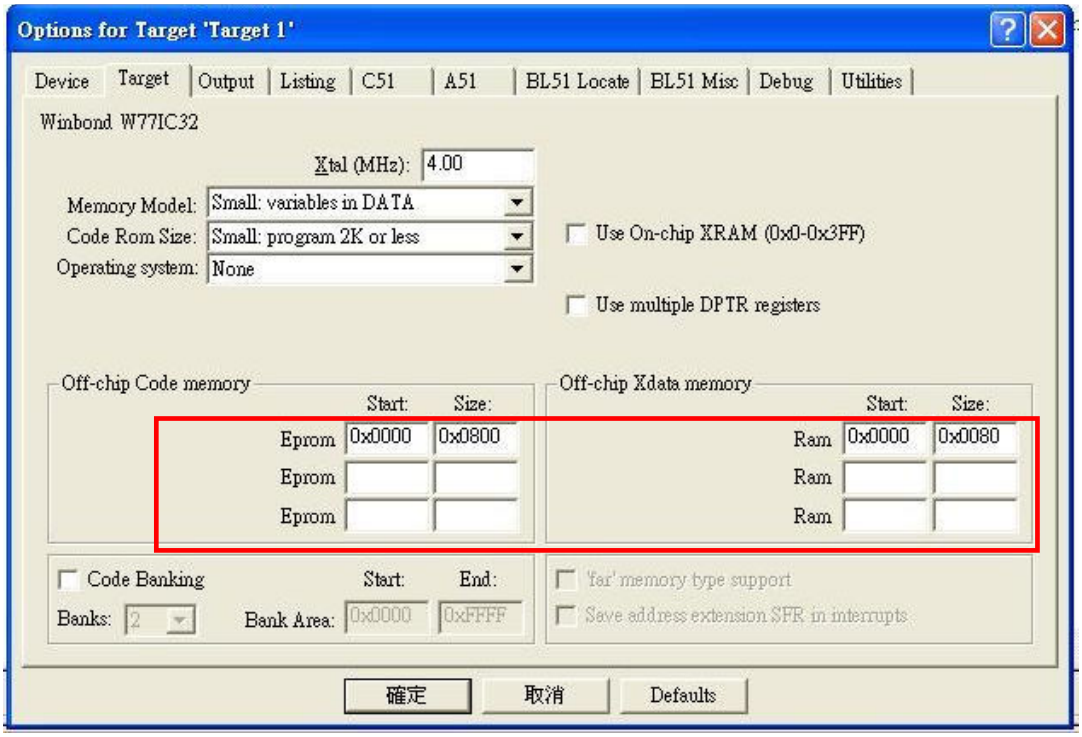
An example on item a is shown below inside the red rectangle:

```
; Main Program
;--------------------------------------
STARTUP:
;--------------------------------
; define option here
; user is prohibited to modify it
#ifndef CHIP
        MOV     0A0H,#0
#endif
        ;----------------------------
        ; if immigrate from DC6688FL32A to DC6688FL16B-E, the following should be added
        MOV     R0,#0FH
        MOV     A,#00111111B
        MOVX    @R0,A

        MOV     R0,#PCCONL
        MOVX    A,@R0
        ORL     A,#11000000B
        MOVX    @R0,A

        ;----------------------------
        ; delay 100ms to let power stable
        ; in case the firmware write data flash at the beginning
        CALL    DELAY

        ;----------------------------
```

For item b, this is a must as on power up, the contents in the SRAM are undetermined.

4 Keil Compiler's environment

When migrating the firmware from DC6688F05S to DC6688F2SCN, some settings in Keil compiler have to modify as shown below highlighted in red box.



5 DEEMAX emulator

5.1 Limitation on DC6688F05S

Before listing the limitation on DC6688F2SCN, we go though on DC6688F05S.

When using emulator, there are some instructions, listed below, that the machine cycle is not identical to that used in our chip.

	Dragonchip	DEEMAX emulator
Mnemonic	Machine cycle	Machine cycle
RET	4	2
RETI	4	2
JMP @A+DPTR	3	2
MOVC A,@A+DPTR	3	2
MOVC A,@A+PC	3	2
INC DPTR	3	2

Additional limitation:

1. Power down mode is not implemented in ICE, don't use it, otherwise, undetermined result occurs.
2. No SL pin on 'J8' in the ICE
3. No XOUT pin on 'J8' in the ICE
4. No watchdog (basic timer) [1]
5. No backup mode
6. No ISP programming
7. Only operated at 3.3V power

Remarks:
[1] don't enable watchdog, otherwise, unexpected result come out.

5.2 Limitation on DC6688F2SCN

Basically, the limitation on DC6688F2SCN is identical to DC6688F05S. Therefore, section 5.1 also applies here.

Those who developed DC6688F05S are suggested to follow the steps below:

1) develop using emulator for DC6688F05S
2) download the firmware to IC(DC6688F05S), and check the prototype.
3) Migrate to DC6688F2SCN according to this document. Develop using emulator for DC6688F2SCN
4) download the firmware to IC(DC6688F2SCN), and check the prototype.

Item 2 above make sure that the major functions work properly
The major function includes:

1) CPU
2) 64B-SRAM

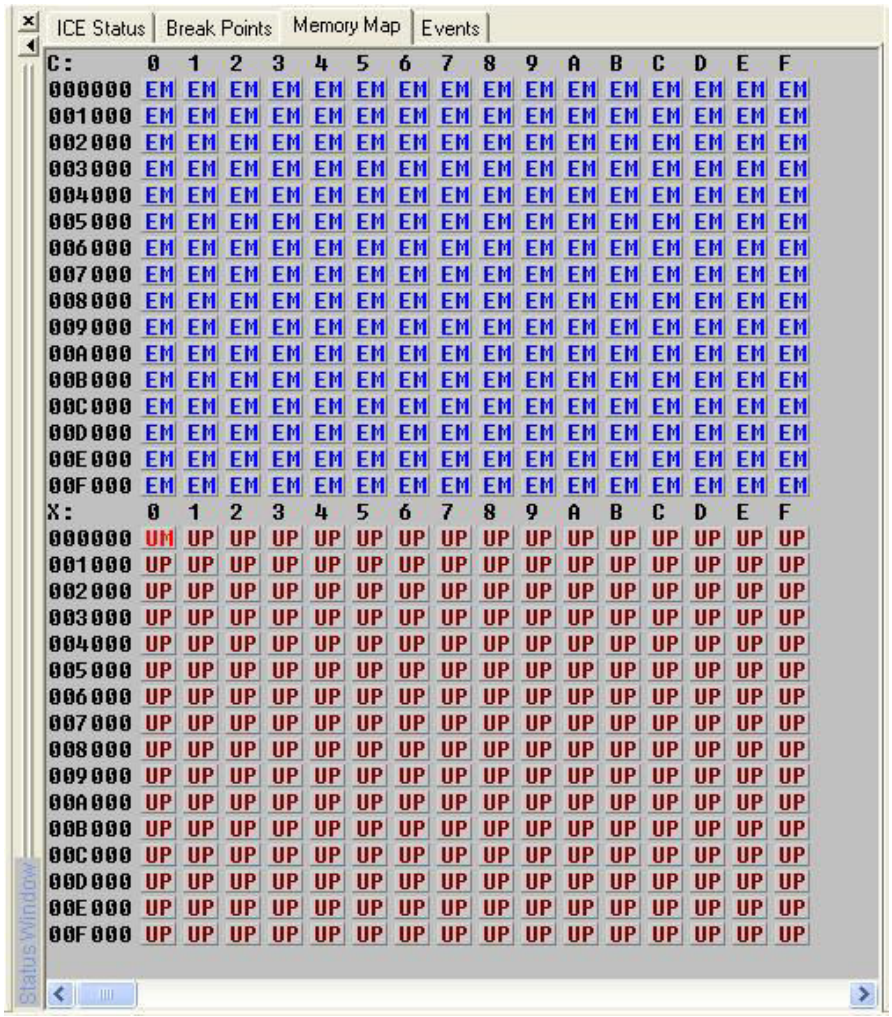
The difference between DC6688F05S and DC6688F2SCN is only on:

1) The ratio of program flash/ROM size.
   DC6688F05S: program flash/ROM = 512B/1.5KB

DC6688F2SCN: program flash/ROM = 2KB/0KB

5.3 Environment setting

In the DEEMAX emulator's software environment, the 'Memory map' in 'Status window' have to modify as shown below:



Copyright Notice

Disclaimer

Dragonchip Ltd. assumes no responsibility for any errors contained herein.

Dragonchip Ltd.
TEL: (852) 2776-0111
FAX: (852) 2776-0996
http://www.dragonchip.com