Dragonchip

AppNote099

Migration from F2SER to F2STR

Document Revision 1.1

January, 2017

Table of Contents

1 Introduction

The objective of this document is to describe the migration from DC6688F2SER to DC6688F2STR.

Two areas will be covered, and explain in detail in the following sections.
1) Development tools
2) Software
3) Hardware

2 Development tools

Before proceeding to software development, make sure the following software components are installed in PC:

1) Keil PK51 v953 or higher

2) Emulator driver v2.6.7 or higher
   Hardware emulator for F2T (DC6688EMT-F2T) must be used.

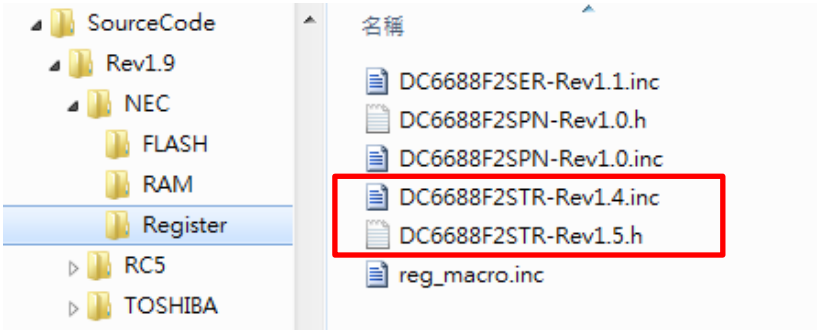
3) Software SLP v6.9.3 or higher
   This is used for production.
   Hardware programming connection refers to section 4.1.

3 Software

For illustration, an example code of remote control for F2STR in Application Note 080 is used.

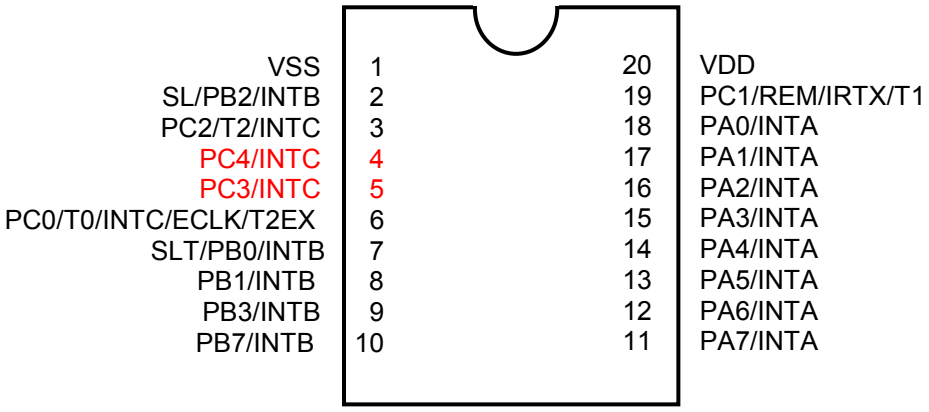
3.1 Header file

The header file for F2STR is available from AppNote080 in c or assembly format as shown below



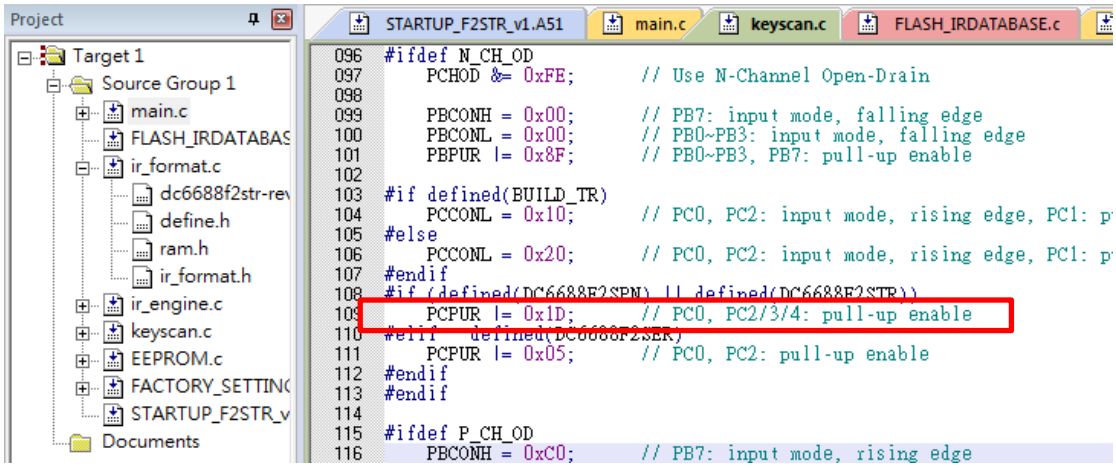
3.2 PC3/PC4 configuration

Since no external resonator is needed, two more I/Os (PC3 / PC4) are available for application as shown below.



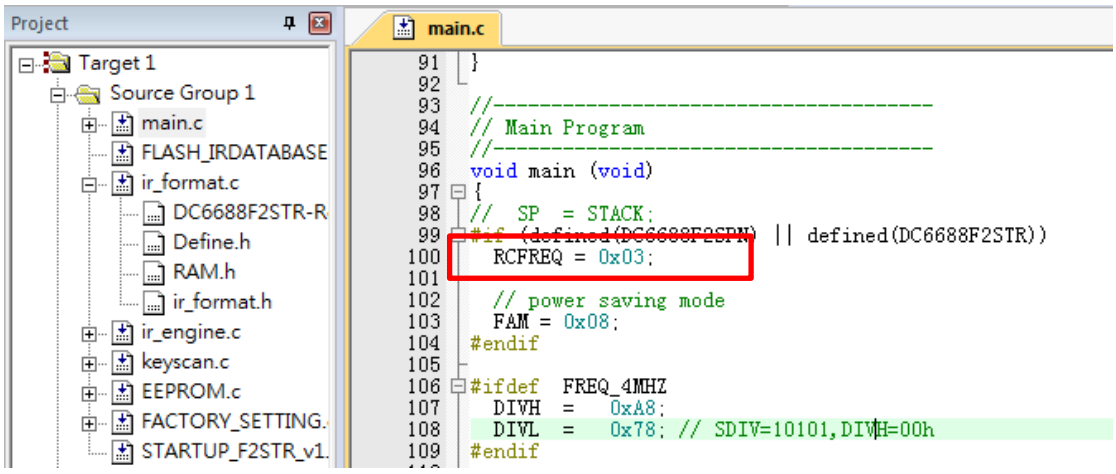
In order to maintain the stop mode current ($Idd_{(pd)}$) within the specification, if those ports are not used, it is required to configure to input with pull-up enable.

An example can refer to function “INIT_2” in file “Keyscan.c”



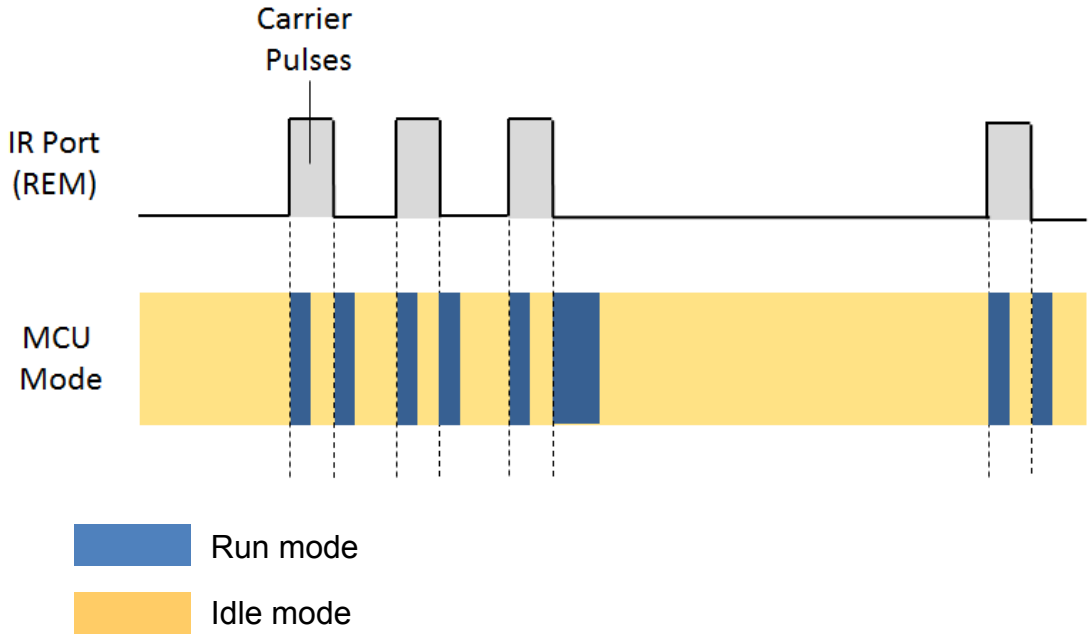
3.3 Internal Frequency 4MHz (default)

The CPU running frequency is set to 4MHz by default.
An example can refer to function “main” in file “main.c” as shown below.



3.4 Idle mode Power saving improvement

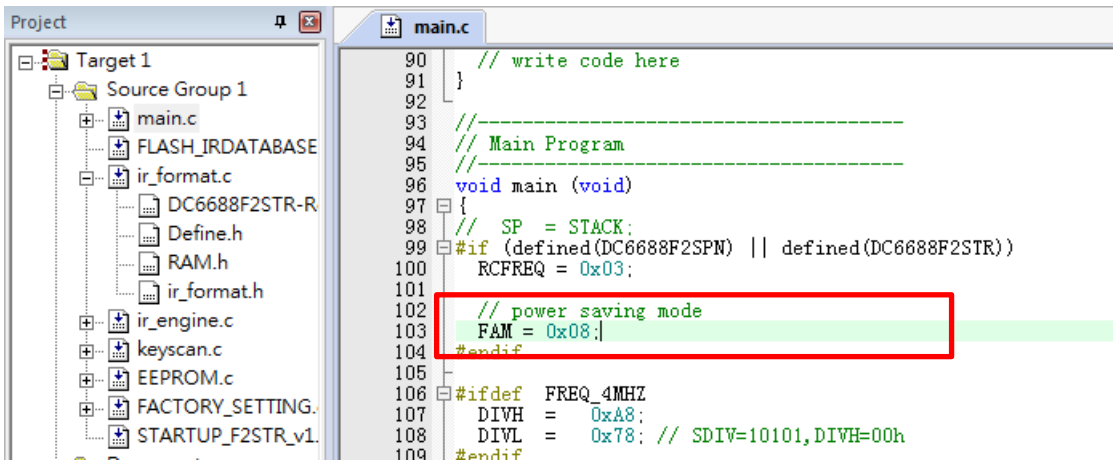
To utilize this feature, idle mode must be enabled in application where possible. An example is shown below. Actually, for remote application when output IR format, the data processing by CPU does not occupy all the time, most of the time can be idle.



Detail can refer AppNote080 example code with user manual showing how to implement.

3.5 Run mode Power saving improvement

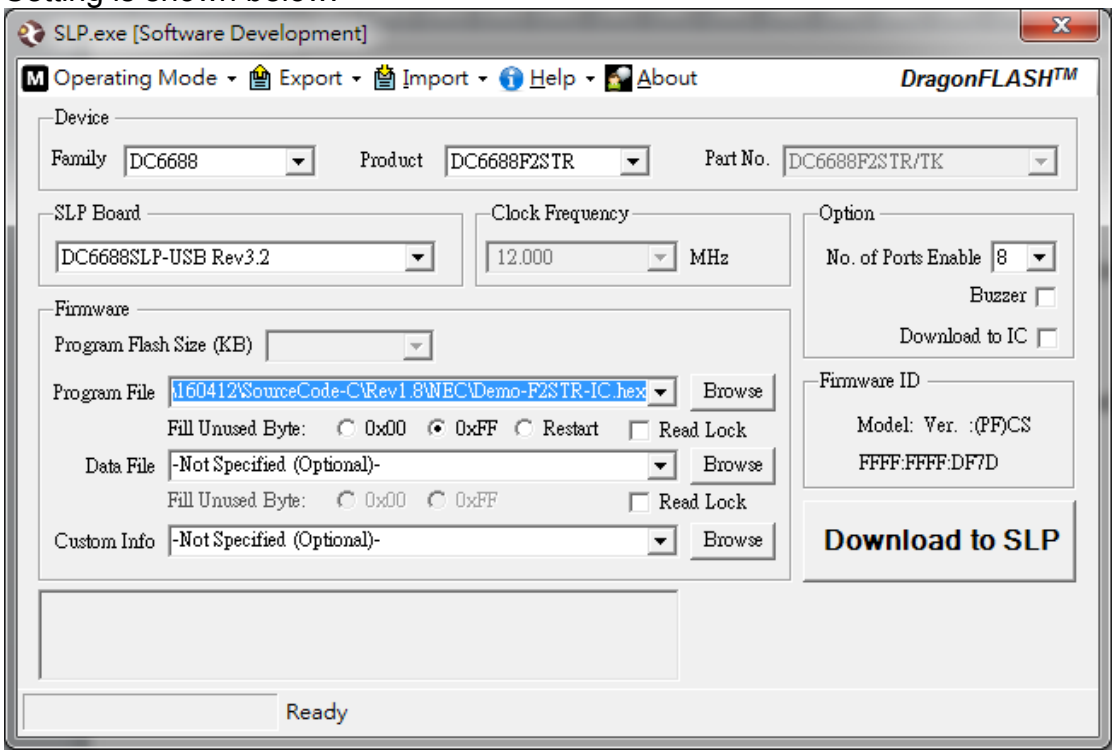
To enable this feature, register 'FAM' must set to 0x08 as shown below.



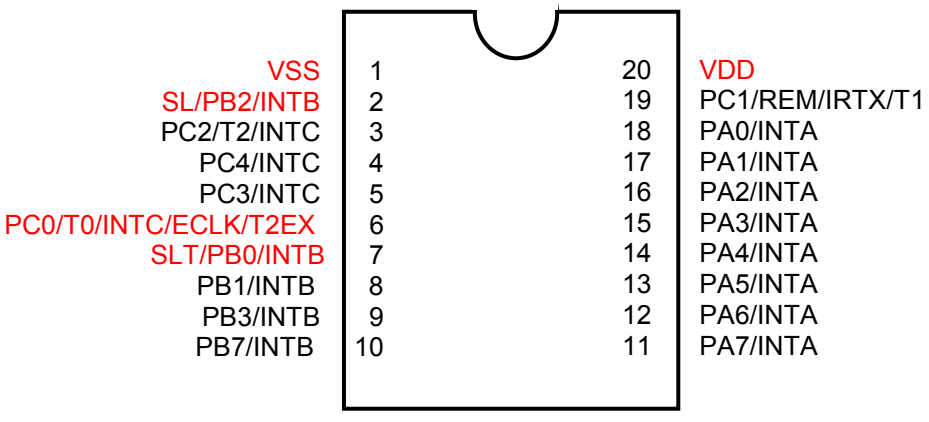
4 Hardware

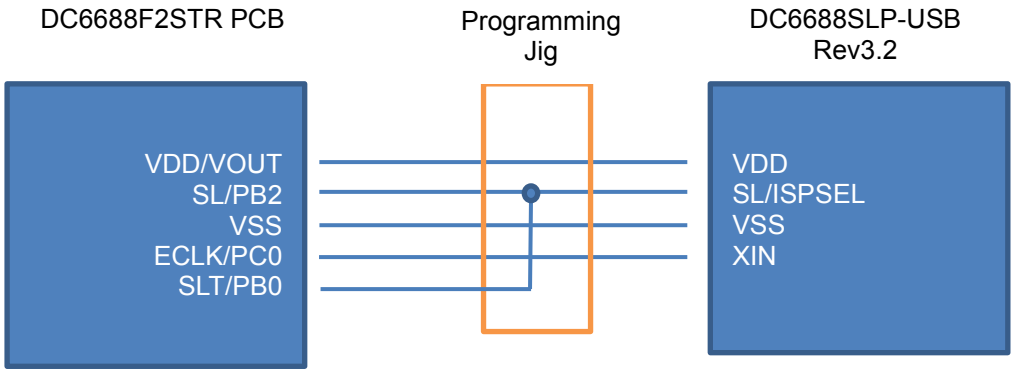
4.1 Programming

The software SLP Rev6.9.3 or higher must be used.
Setting is shown below:

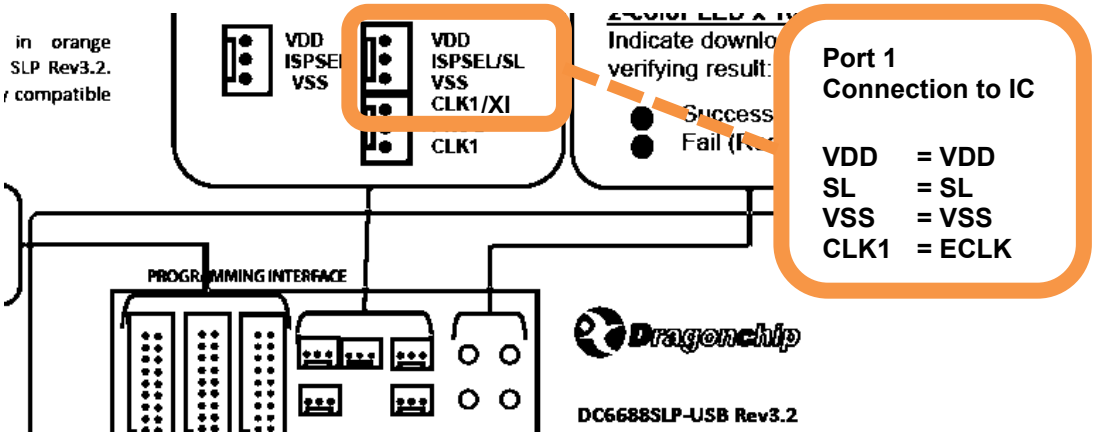


The programming pin is highlighted below.

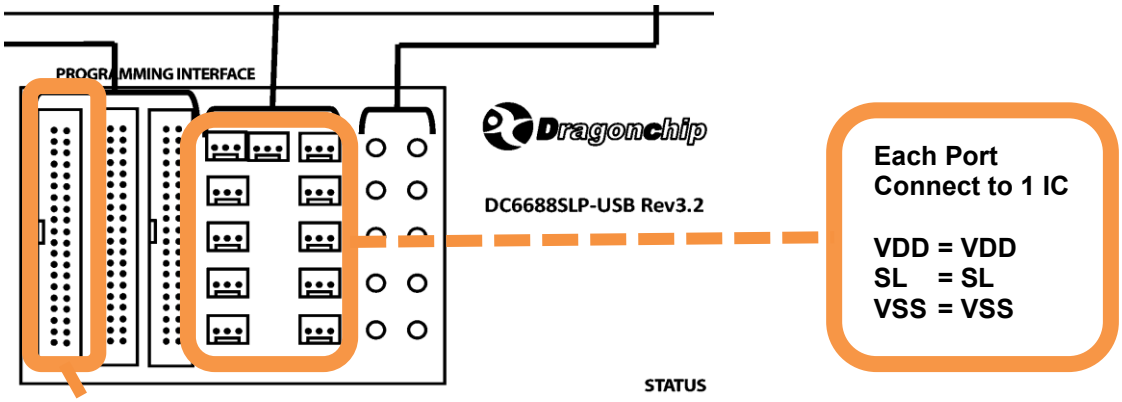




1) Single Device Programming



2) Multiple Devices Programming



J26 Pin Assignment

Pin	Name	Connection	Pin	Name
1	LCD_P	LCD module pin 9 (DB2)	2	GND
3	LCD_P8	LCD module pin 8 (DB1)	4	LCD_P10
5	LCD_P7	LCD module pin 7 (DB0)	6	LCD_P11
7	LCD_P6	LCD module pin 6 (E)	8	LCD_P12
9	LCD_P5	LCD module pin 5 (R/W)	10	LCD_P13
11	LCD_P4	LCD module pin 4 (RS)	12	LCD_P14
13	LCD_P3	LCD module pin 3 (VEE)	14	LCD_P15
15	LCD_P2	LCD module pin 2 (VCC)	16	LCD_P16
17	LCD_P1	LCD module pin 1 (VSS)	18	GND
19	GND	GND	20	NC
21	CLK1	D1 XIN/ ECLK pin	22	GND
23	CLK2	D2 XIN/ ECLK pin	24	GND
25	CLK3	D3 XIN/ ECLK pin	26	GND
27	CLK4	D4 XIN/ ECLK pin	28	GND
29	CLK5	D5 XIN/ ECLK pin	30	GND
31	CLK6	D6 XIN/ ECLK pin	32	GND
33	CLK7	D7 XIN/ ECLK pin	34	GND
35	CLK8	D8 XIN/ ECLK pin	36	GND
37	CLK9	D9 XIN/ ECLK pin	38	GND
39	CLK10	D10 XIN/ ECLK pin	40	GND

Each XIN pin for 1 IC's ECLK

Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	Jan 2017			Preliminary	Danny Ho	Patrick Li

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