Dragonchip

Single Remote Control application using DC6688F2P Voltage-doubler

AppNote119

Document Revision 1.2

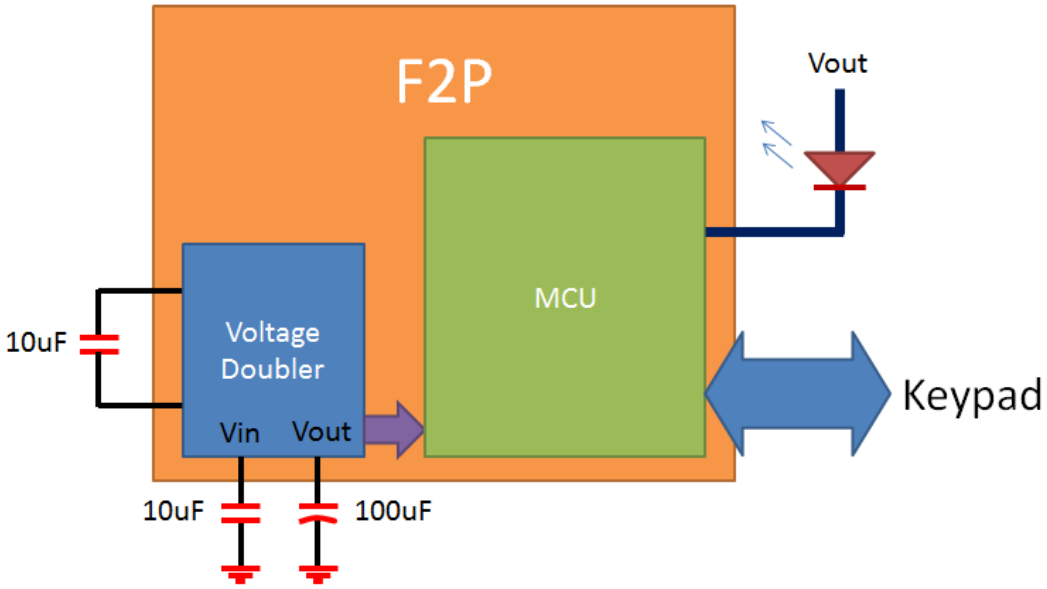
October, 2018

Table of Content

1 Introduction

The objective of this document is to provide technical information on making the remote using DC6688F2P.

A block diagram of F2P voltage-doubler for remote control application is shown below.



A BOM is listed below:

Item	Quantity
DC6688F2P	1
IR diode	1
Capacitors	4
Battery clip	1

Three areas will be covered, and explain in detail in the subsequent sections.
1) Development tools
2) Software
3) Hardware

2 Development tools

Before proceeding to software development, make sure the following software components are installed in PC:

1) Keil PK51 v953 or higher

2) Emulator driver v3.1.2 or higher
   Hardware emulator for F2P (DC6688EMT-F2T) must be used.

3) Software SLP v8.2.1 or higher
   This is used for production.
   Hardware programming connection refers to section 4.1.

3 Software

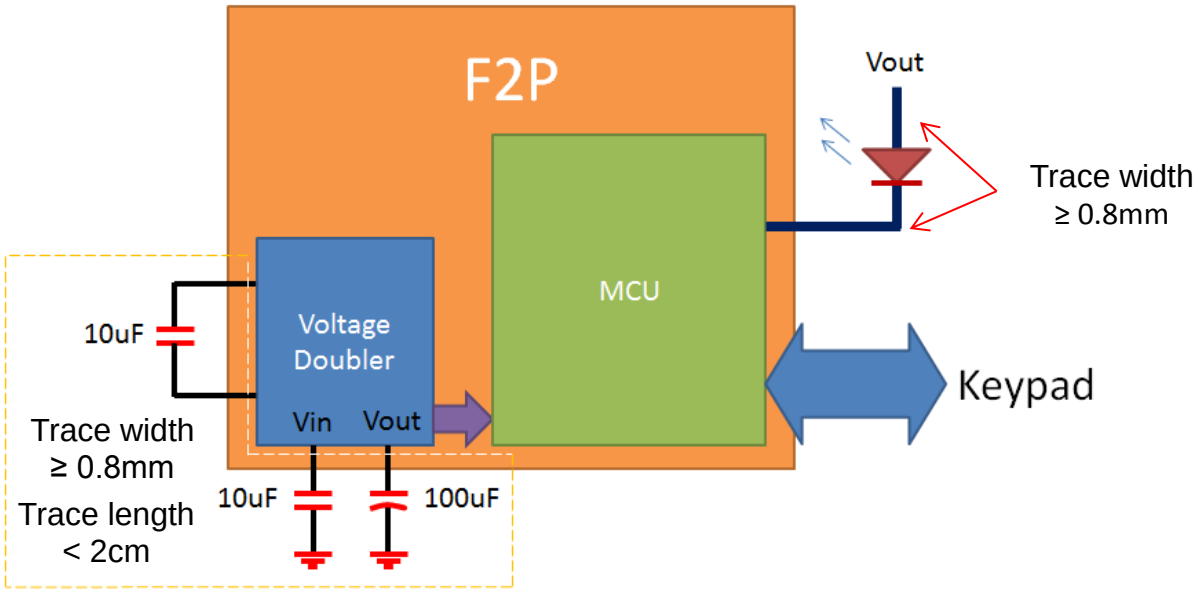
Detail refers AppNote080, in which an example code of remote control for F2P is prepared.

4 Hardware

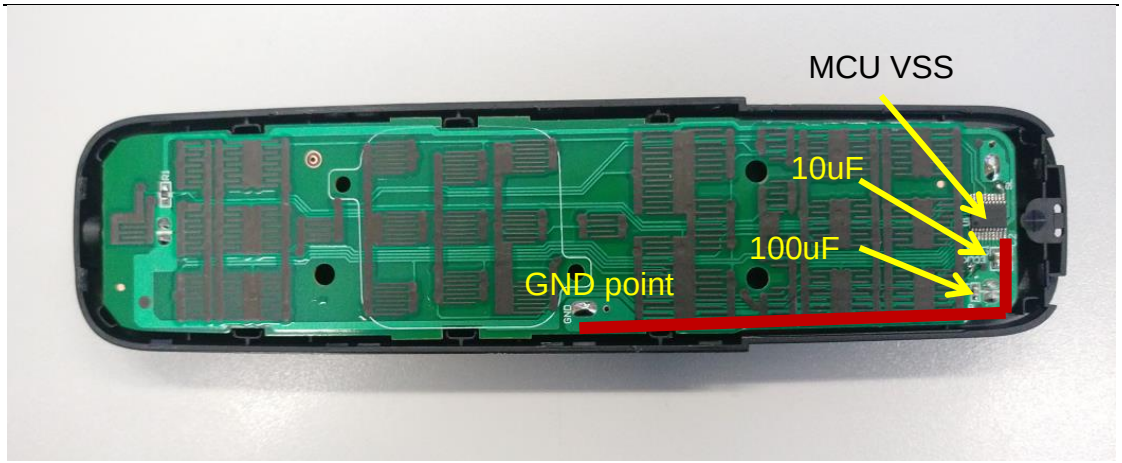
4.1 PCB Layout

There are two areas need to pay attention:

1. The path on IR diode
   1.1 Trace width must be larger than 0.8mm
2. The circuit on voltage doubler
   2.1 All the capacitors connected to the voltage doubler should be placed as close as possible to the IC. Trace length within 2cm is recommended.
   2.2 Trace width must be larger than 0.8mm
   2.3 Multilayer ceramic caps (±10%)

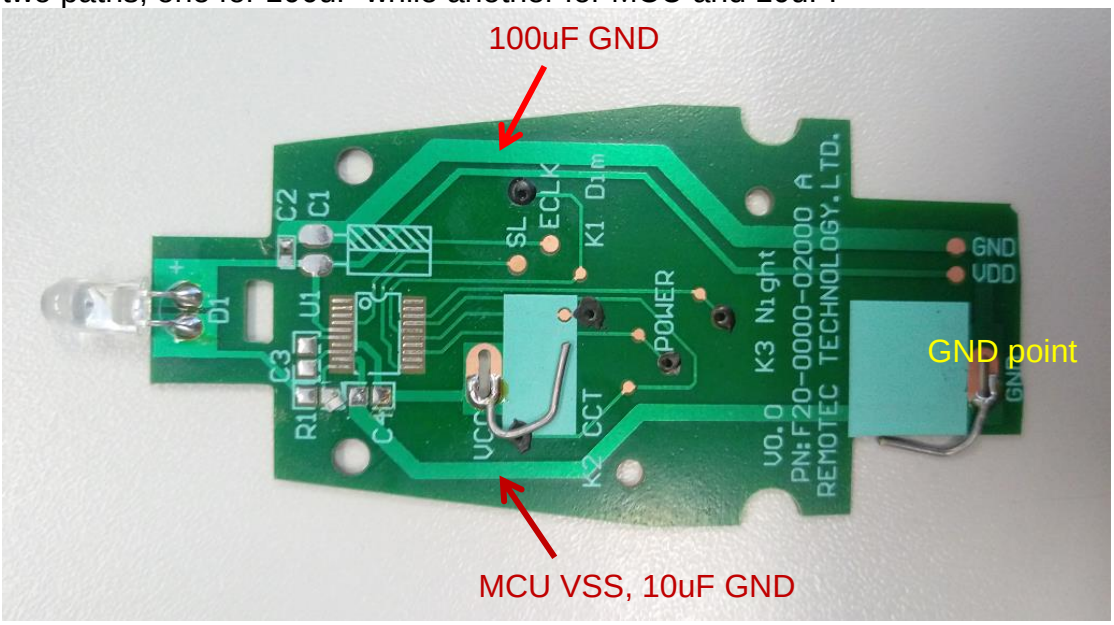


3. All capacitors and MCU VSS should be on one ground line
   Below shows an example of good and bad layout.
   3.1 Good layout



3.2 Bad layout

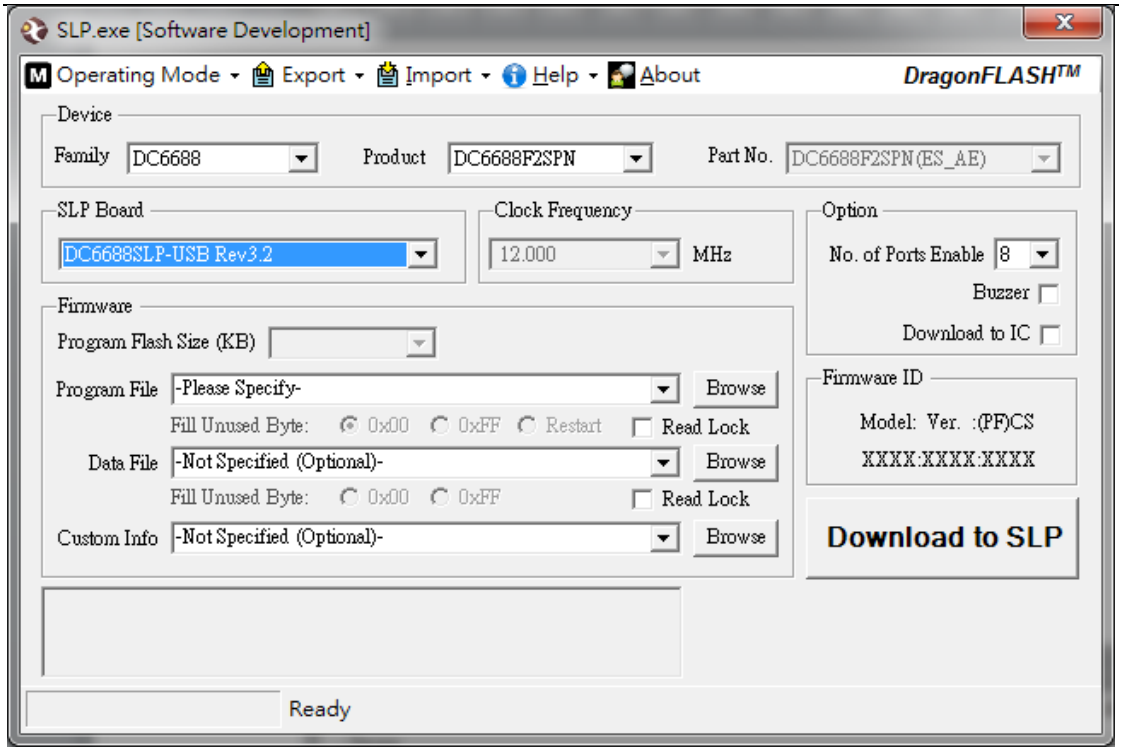
The layout below is considered to be bad as ground (GND) is separated into two paths, one for 100uF while another for MCU and 10uF.



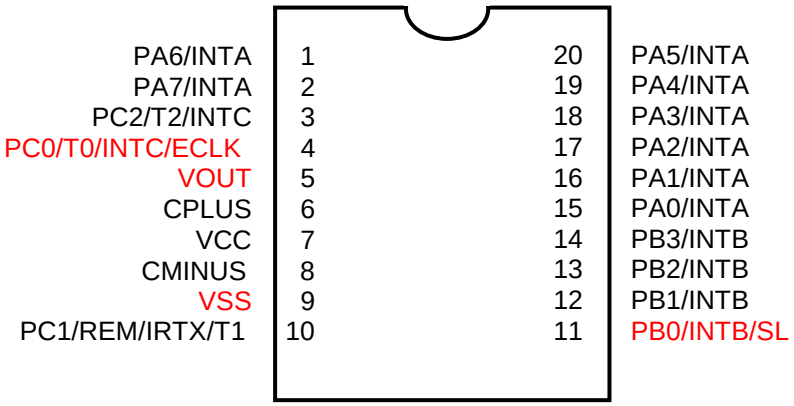
4. No carbon film is allowed between IC and programming pad
   Carbon film resistance would affect the signal integrity, and therefore, is prohibited

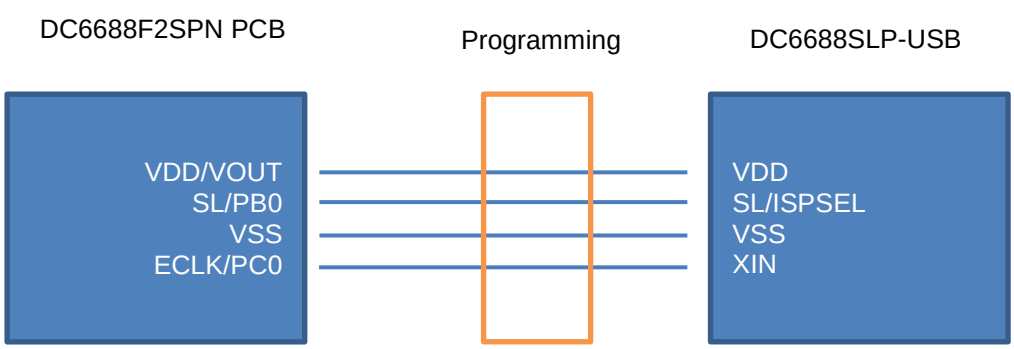
4.2 Programming

The software SLP Rev6.9.3 or higher must be used.
Setting is shown below:

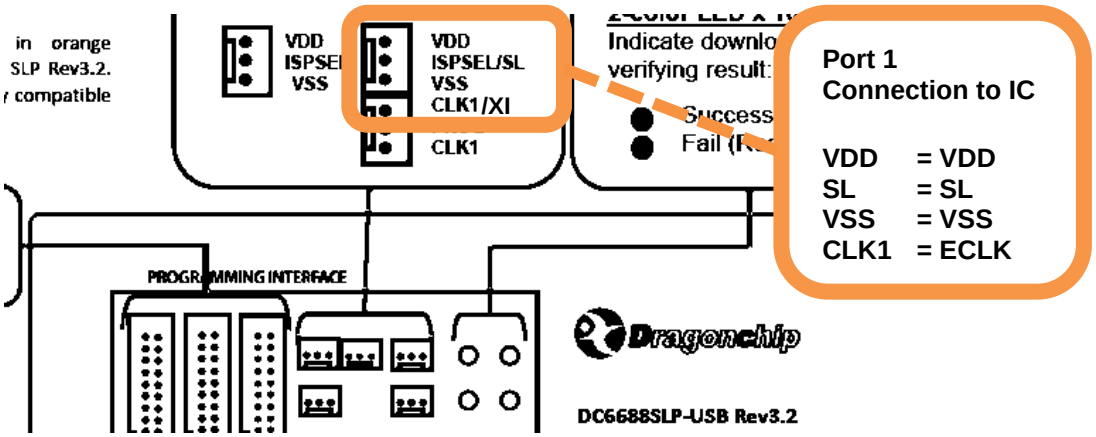


The programming pin is highlighted below.

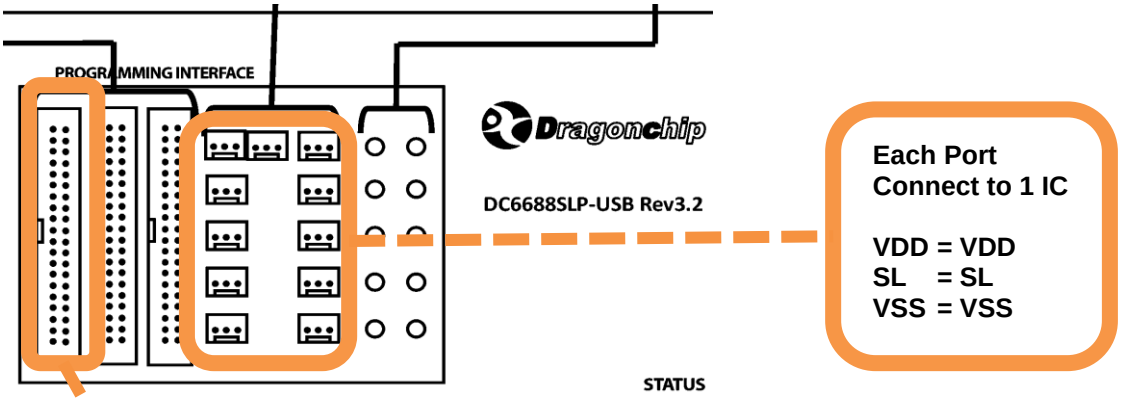




1) Single Device Programming



2) Multiple Devices Programming



J26 Pin Assignment

Pin	Name	Connection	Pin	Name
1	LCD_P	LCD module pin 9 (DB2)	2	GND
3	LCD_P8	LCD module pin 8 (DB1)	4	LCD_P10
5	LCD_P7	LCD module pin 7 (DB0)	6	LCD_P11
7	LCD_P6	LCD module pin 6 (E)	8	LCD_P12
9	LCD_P5	LCD module pin 5 (R/W)	10	LCD_P13
11	LCD_P4	LCD module pin 4 (RS)	12	LCD_P14
13	LCD_P3	LCD module pin 3 (VEE)	14	LCD_P15
15	LCD_P2	LCD module pin 2 (VCC)	16	LCD_P16
17	LCD_P1	LCD module pin 1 (VSS)	18	GND
19	GND	GND	20	NC
21	CLK1	D1 XIN/ ECLK pin	22	GND
23	CLK2	D2 XIN/ ECLK pin	24	GND
25	CLK3	D3 XIN/ ECLK pin	26	GND
27	CLK4	D4 XIN/ ECLK pin	28	GND
29	CLK5	D5 XIN/ ECLK pin	30	GND
31	CLK6	D6 XIN/ ECLK pin	32	GND
33	CLK7	D7 XIN/ ECLK pin	34	GND
35	CLK8	D8 XIN/ ECLK pin	36	GND
37	CLK9	D9 XIN/ ECLK pin	38	GND
39	CLK10	D10 XIN/ ECLK pin	40	GND

Each XIN pin for 1 IC's ECLK

Please refer to SLP Rev3.2 manual for more details.

Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	Apr. 2017			Preliminary	Danny Ho	Patrick Li
1.1	Nov, 2017	4		Added description on layout	Danny Ho	Patrick Li
1.2	Oct, 2018	4		Added description on layout	Danny Ho	Patrick Li
		2		Driver version update		

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