Dragonchip

DC6688WF Application Guide

AppNote132

Document Revision 1.5

July, 2019

Table of Content

1 Introduction

The Objective of this document is to provide the user on the following area no matter it is module-based or embedded in application board:

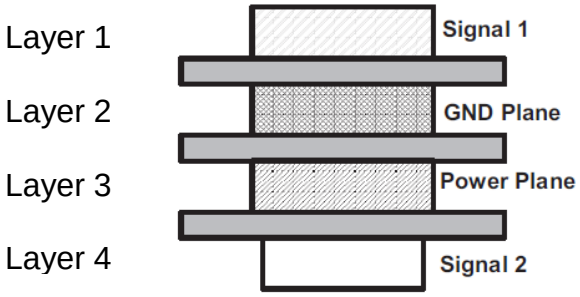
1) Layout Guide
2) RF Tuning Guide
3) Troubleshoot Guide
4) Application circuit Guide
5) Firmware update via OTA

2 Layout Guide

FR4 4-layer PCB is recommended.

2.1 Board Stack-up

Four-layer Board Stack-up is shown below.

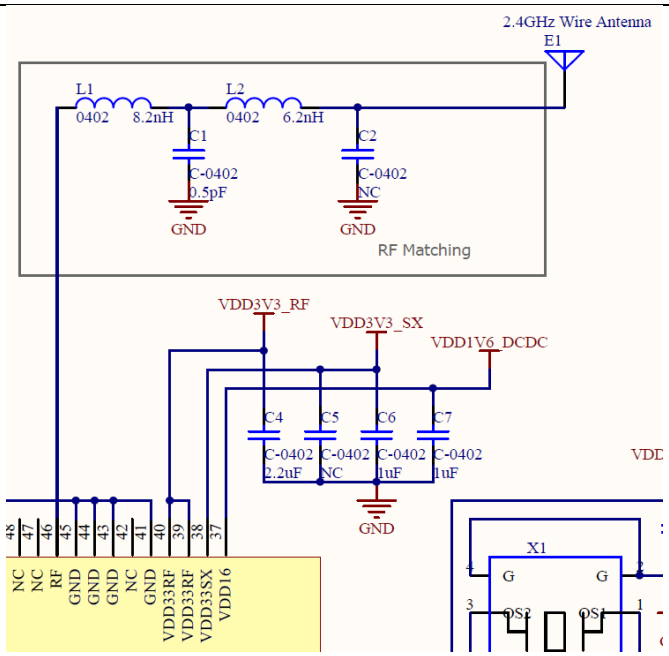


To maximize the performance, GND copper pour is a must where applicable in any layer.

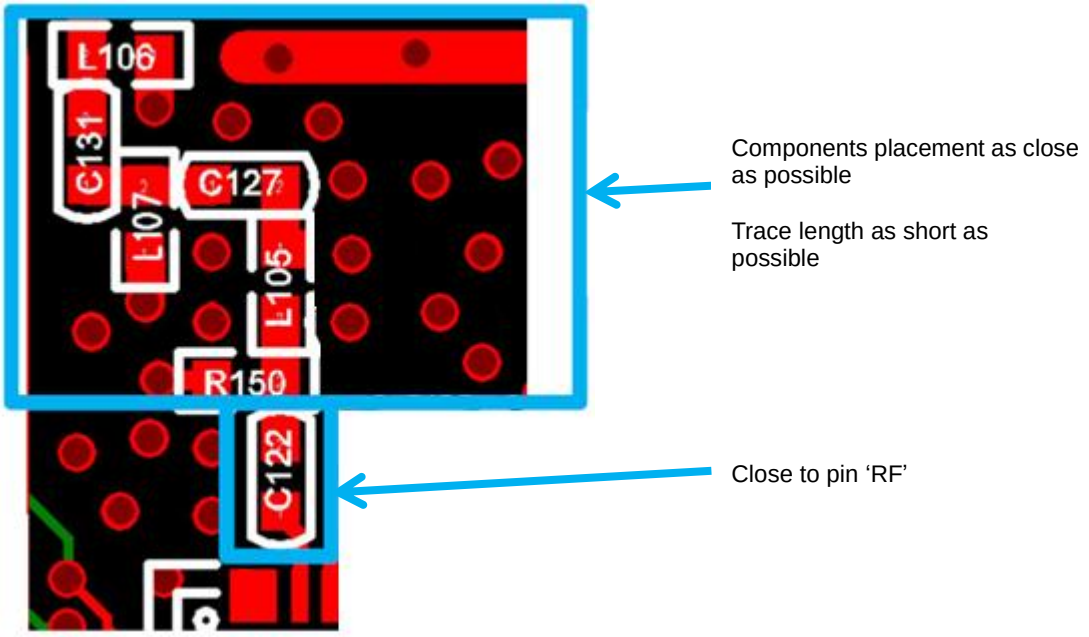
The majority of signal traces should run on a single layer, preferably SIGNAL1. Immediately next to this layer should be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

2.2 RF pin (pin 46)

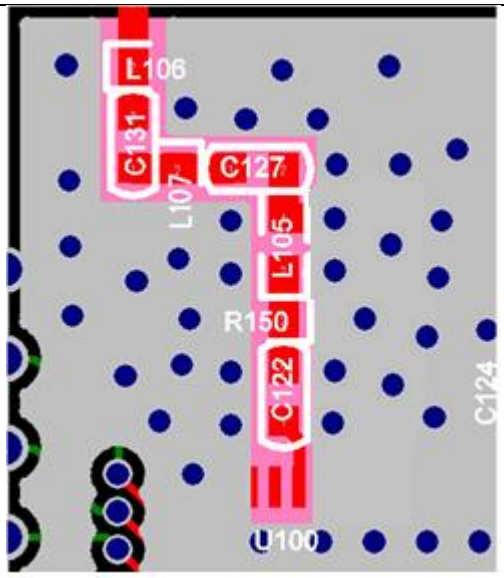
1. L1 component should be placed as close as possible to the pin ‘RF’.



2. All the components on the RF matching circuit should be placed as close as possible. Trace length should also be kept as short as possible.



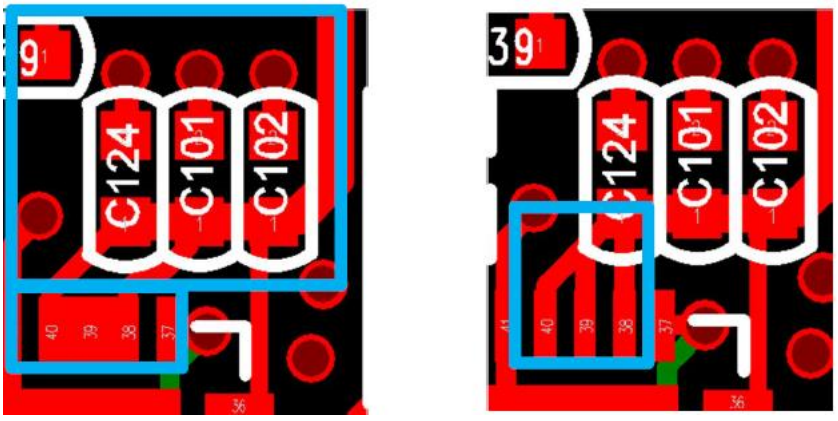
3. Bypass capacitor must be placed as close as possible to the chip. Trace length should also be kept as short as possible.
4. Keep the RF trace at 50 Ω (critical).
5. The layer 2 of PCB prefers ground plate. Using the lower layer (main PCB ground plane) for ground return increases the loop inductance
6. The path though out the RF matching circuit on top layer (layer 1) must be a keep-out area which cannot be routed by any signal on layer 2.



7. The trace width though out the RF matching circuit must be the same as the pad width.
8. Connect the IC ground pins and bypass capacitors' ground pads directly to the ground on Layer 2 using micro-vias at each pin or pad (critical).

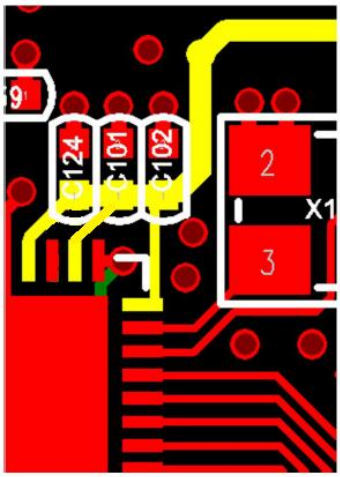
2.3 VDD33RF pin (Pin 39/40)

Pin 36, 38, 39, 40 must route to decoupling cap with its own trace separately.

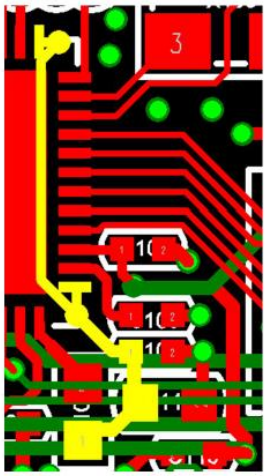


Good Bad

VDD33 (pin 36, 38, 39, 40) trace width recommends 15mil
VDD16 (pin 25, 37) trace width recommends 8-12mil.

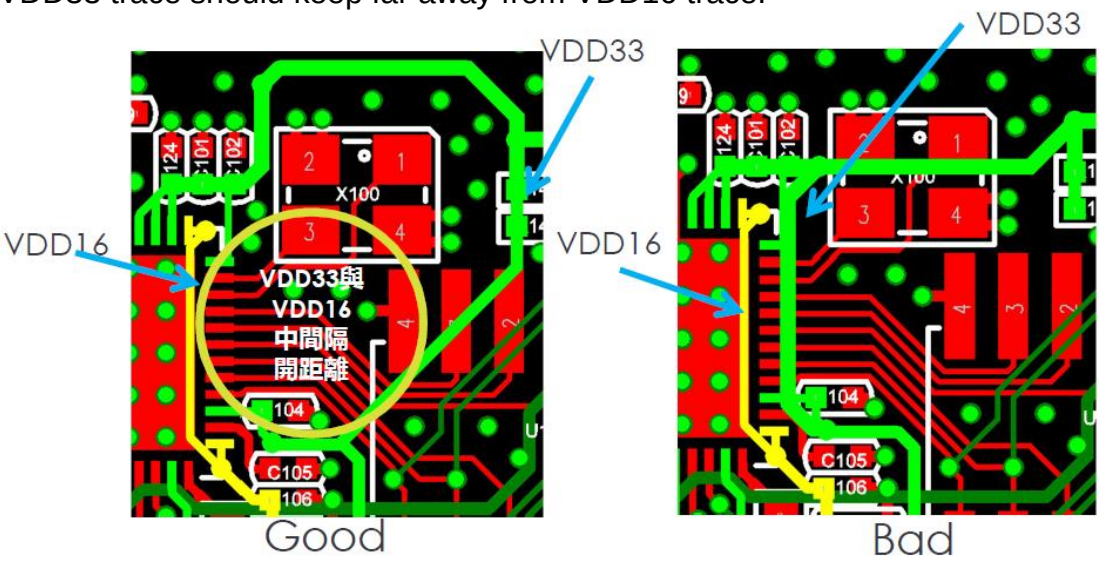


VDD33



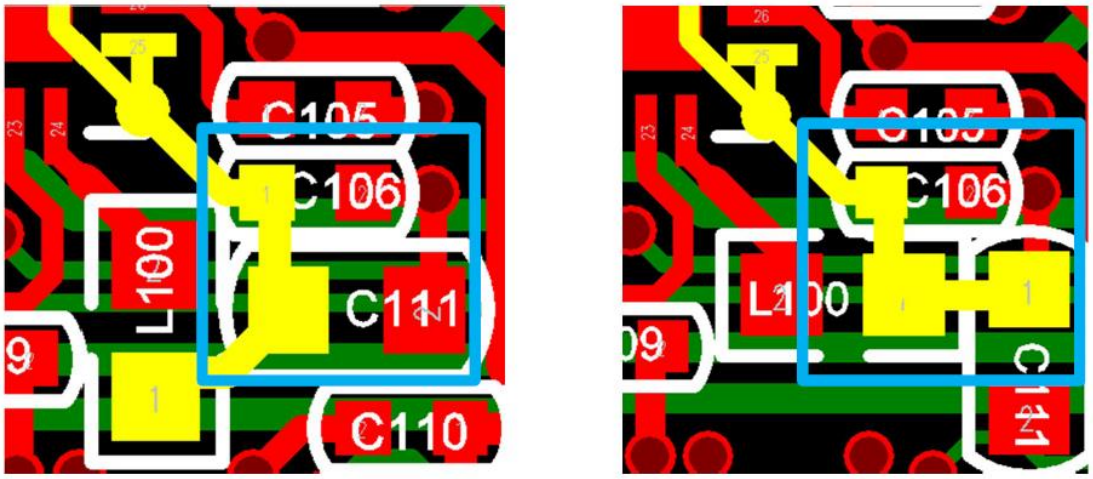
VDD16

VDD33 trace should keep far away from VDD16 trace.

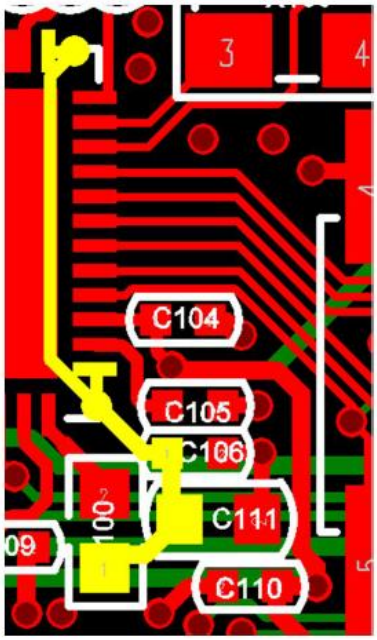


2.4 VDDLXDC pin (Pin 24)

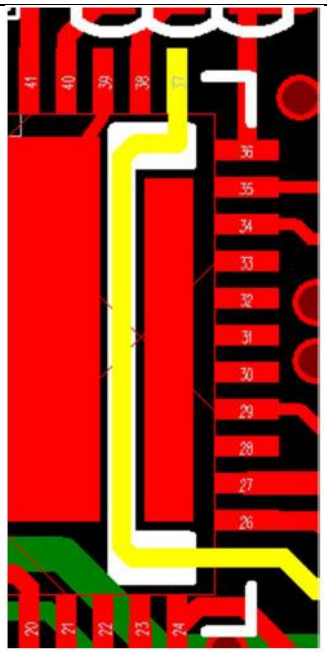
Pin 24 (VDDLXDC) should go through inductor before decoupling cap to pin 25 (VDD16DC), and route to pin 37 (VDD16) though layer 4.



VDD16 trace should keep away from pin 29.

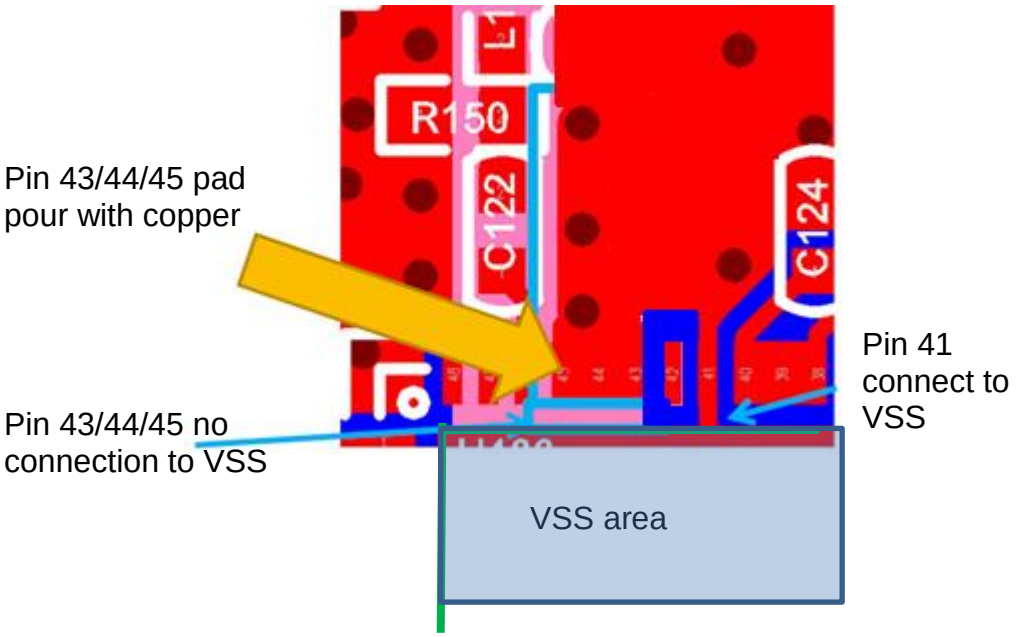


If using two-layer PCB, VDD16 trace must route underneath the package to keep away from pin 34, 35 oscillation, and white coating is necessary for electrical isolation.



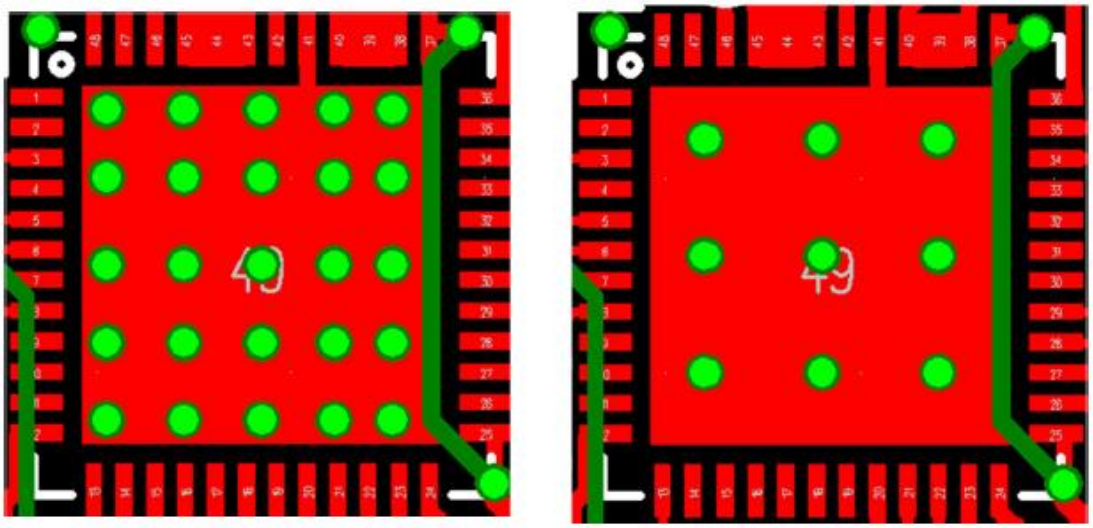
2.5 GND pin

- Pin 43/44/45 pad must be poured with copper to inter-connect each other.
- Pin 43/44/45 must have big GND PAD, at least 3 via to GND layer
- Pin 43/44/45 are not allowed to connect with E-PAD (VSS)
- Only pin 41 connect to E-PAD (VSS)



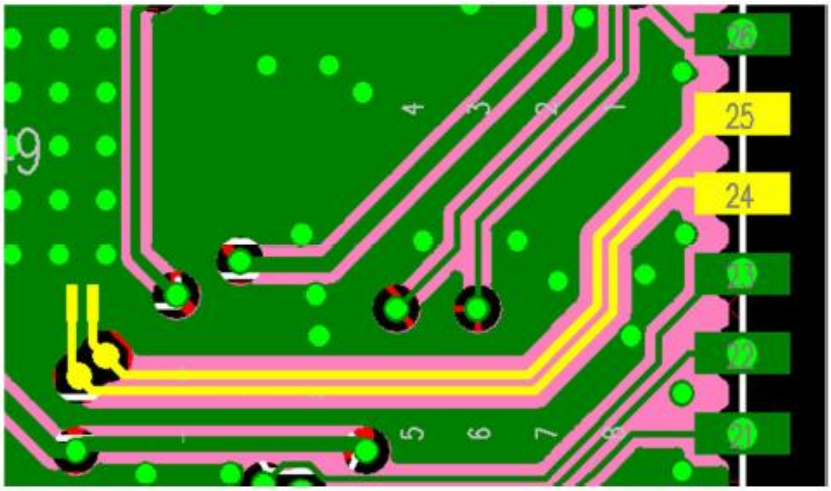
2.6 VSS pin (E-PAD)

VSS (E-PAD) must have enough via to GND layer.



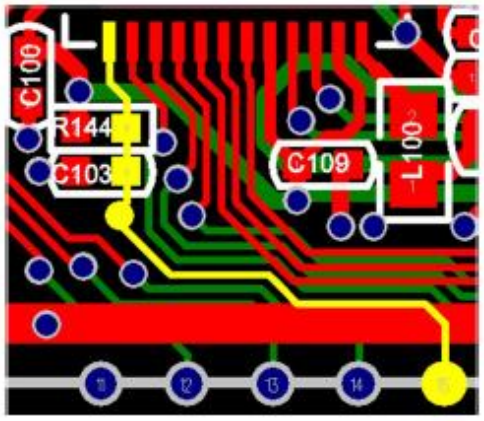
2.7 HSDP/HSDM (Pin 21/22)

- The traces should always be matched lengths and must be no more than 4 inches in length.
- Route the traces close together for noise rejection on differential signals, parallel to each other and space within two mils in length of each other (start the measurement at the chip package boundary, not to the balls or pins).

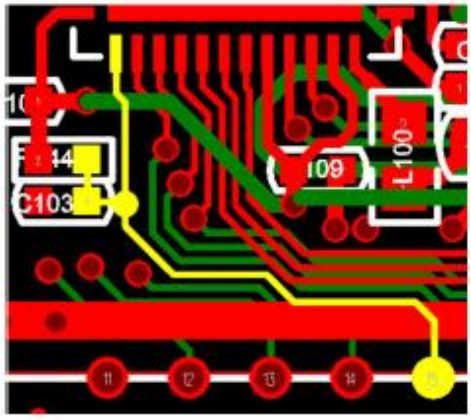


2.8 LDO_EN (Pin 13)

'LDO_EN' pin should go through the pad of R/C components directly prior to the module pin.



Good



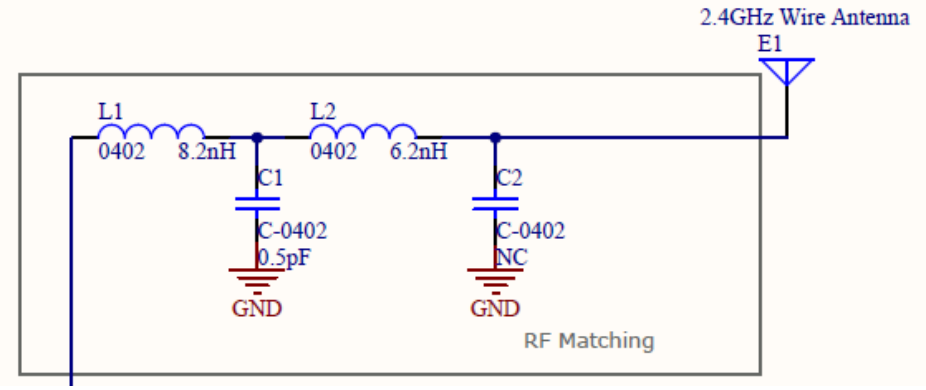
Bad

2.9 Crystal

The crystal should be placed as close as possible to pin 34/35. The trace and its pads should be enclosed by GND on layer 1 to avoid crosstalk to other pins.

3 RF Tuning Guide

L2 initial value recommends 6.2nH
Keep the RF trace at 50 Ω



C1 initial value: 0.5pF, adjustable range from 0.5pF ~ 1pF
L1 initial value: 8.2nH, adjustable range from 6.2nH ~ 9.1nH
During adjusting L1 and C1, keep monitoring the changes of Power/EVM/2nd harmonic.

4 Troubleshoot Guide

4.1 Boot-strapping check

GPIO14 / GPIO15 should be NC when power up for the right boot-strapping configuration.

4.2 Xtal Freq. check

Make sure the setting in bin file matching with the crystal frequency used on the board.

4.3 Power check

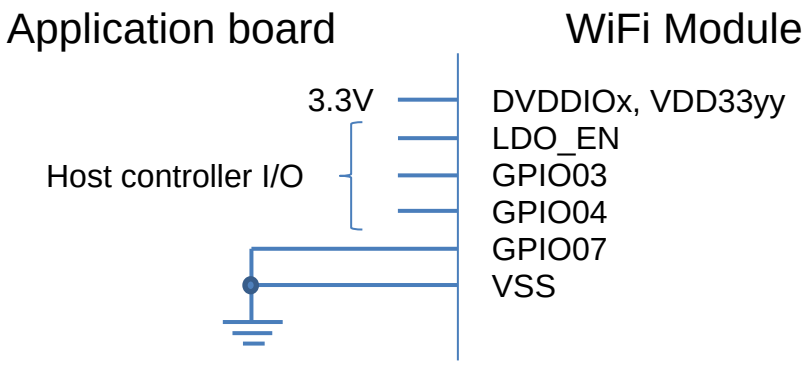
1. Make sure 3.3V applied to VDD (pin 12, 20, 23, 26, 36, 38, 39, 40) on board.
2. Check 1.6V whether present or not on VDD16 (pin 25, 37). If not, check L and C components across pin 24 and 25.

4.4 Firmware check

1. After power up, check clock output on GPIO15.
2. GPIO07 should be pull-low all the time in application. Upon power up, Debug information would be output on GPIO04. AT command should be available as well.

5 Application circuit Guide

Below diagram shows the minimum connection to the application board from WiFi Module.



5.1 AT-command port

The AT-command is implemented through UART communication on the following ports to the host controller or WiFi tester:

1) GPIO03
   甲、RX
2) GPIO04
   甲、TX

In production, WiFi tester can communicate with DC6688WF through this port. If WiFi have to be tested in customer production lines, then, pads must be reserved on PCB such that test probe can connect them to the tester, and the host controller should configure the port to Hi-Z to release to the WiFi tester.

5.2 LDO_EN pin

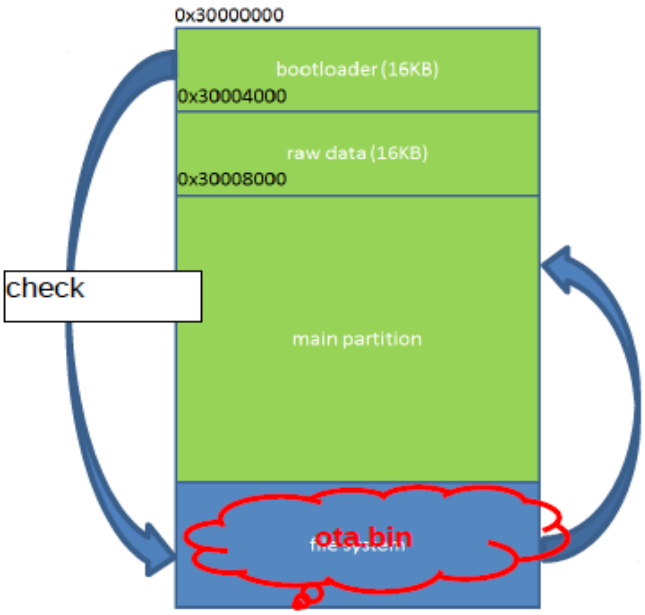
This pin serves two purposes:

1) Power saving
   甲、To save the power, asset this pin to low. The core will shut down.
2) Reset WiFi
   甲、To reset the WiFi, send a negative pulse to this pin. The core will shut down and then, restart to run the firmware.

6 Firmware update via OTA

6.1 OTA Flow

1. Download the firmware file through OTA API over the cloud. The file will be stored in file system.
2. After download, the file integrity will be checked with md5 checksum. 'Verify SUCCESS' will be displayed if check complete.
3. The system will auto-restart if 'Verify SUCCESS', otherwise, jump to old firmware in main partition to run the application.
4. The bootloader check if new firmware is found to do update
5. The new firmware copy to main parttion.



6.2 OTA API

1. OTA support http & tftp
2. API example
- HTTP usage
    -- AT+OTASETSERVER=192.168.2.77,80,0 (Server IP, Port Number, Protocol HTTP : 0)
    -- AT+OTASETPARAM=chocolate,/ota/ (OTA File Name, File Path)

-- AT+OTASTART

- TFTP usage

-- AT+OTASETSERVER=192.168.2.156,69,1 (Server IP, Port Number, Protocol TFTP : 1)

-- AT+OTASETPARAM= chocolate (OTA File Name, File Path : NULL)

-- AT+OTASTART

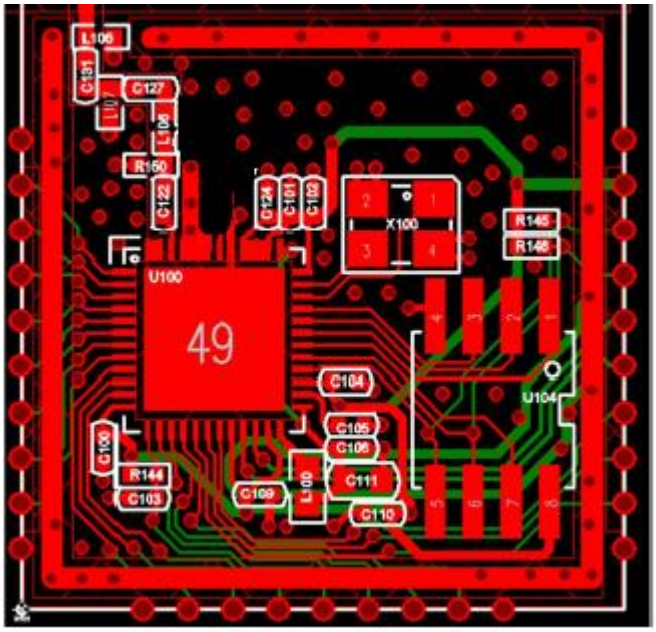
6.3 Firmware file path

The latest firmware is located in our server, and available to download:
1) Bin file
http://file.dragonchip.com/tmplinks/DC6688WF/mac_atcmd.bin

AT command refers to AppNote133.

7 WiFi Module reference

An example of module board for IoT application is shown below.



Revision History

Document Rev. No.	Issued Date	Section	Page	Description	Edited By	Reviewed By
1.0	May, 2019	All		Preliminary	Danny Ho	Patrick Li
1.2	June, 2019	3, 4		Update description	Danny Ho	Patrick Chan
1.3	July, 2019	4.4		Update description	Danny Ho	Patrick Chan
1.4	July, 2019	5, 6		Add new section	Danny Ho	Patrick Chan
1.5	July, 2019	6		Add description	Danny Ho	Patrick Chan

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