DC6288FD

Mixed-Signal LCD Flash Microcontroller

DC6288FD is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory and LCD driver. It is manufactured in advanced CMOS process with Super 1T CISC CPU core, Flash memory, and digital and analog peripherals suitable for mixed-signal application. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T CISC 8-bit CPU core
  - 12MHz, 1 MIPS/MHz
  - 4 priority level interrupt controller
- Application Memory
  - 256B core SRAM with 2 KB Expanded SRAM
  - 32 KB Configurable Program & Data Flash Memory
  - Self-Flash memory read/write with write protection mechanism
- Built-in LCD Controller / Driver
  - Support 4COM or 8COM
  - 224 pixels (28 seg x 8 com)
  - 288 pixels (36 seg x 8 com)
  - 416 pixels (52 seg x 8 com)
- Clocks
  - High accuracy 12MHz oscillator
  - Low power 50kHz oscillator
- Up to 50 GPIO with interrupt function
- Timers/Counters/Pulse Width Modulators
  - 16-bit Timers x 2
  - 16-bit Timer with 4 compare/capture modules supporting motor control
  - 24-bit Timer with 3 compare modules supporting motor control
  - 16-bit Watchdog Timer x 1
  - 8-bit Pulse width modulator x 2
  - 20-bit RTC Timer
- 12-Bit Full-differential ADC with single-end input mode
  - Maximum 200k samples per second
  - 20 input channels
  - Window comparator
  - Temperature Sensor
  - Bandgap Voltage Reference
- Communication Interfaces
  - Integrated Enhanced USART x 1
  - Synchronous Serial Interface (SPI)
  - I^2C with support for SMBus
- Power Monitor
  - Low Voltage Detection (LVD) BOR
  - 4 selectable levels of Low Voltage Indication (LVI)
- Support OTA through UART
- Support on-chip debug and C development
- Operating voltage: 1.5 - 3.6V
- LCD Auto-run mode for low stand-by current consumption (<20uA)
- Temperature range: -40 to 85, 105°C
- Package type:
  - 56-pin QFN 8mm x 8mm, 0.5mm pitch
  - 88-pin QFN 10mm x 10mm, 0.4mm pitch
  - 128-pin LQFP 14mm x 14mm, 0.4mm pitch
  - 128-pin QFN 14mm x 14mm, 0.4mm pitch

  Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

T_A = 25°C, unless specified otherwise

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B,C and D[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B,C and D[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Junction Temperature Range	T_J	-	-40 to +105	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:

[1] It is measured for any one of I/O pin when configured to push-pull output high.

[2] It is measured as total for Ports A, B, C and E when configured to push-pull output high.

[3] It is measured for any one of I/O pin when configured to push-pull output low.

[4] It is measured as total for Ports A, B, C and E when configured to push-pull output low.

1.2 DC Electrical Characteristics

T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V, unless specified otherwise

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input pins except XIN2	0.7 V_{DD}	-	V_{DD}	V
	V_{IH2}	XIN2	V_{DD} - 0.3	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins except XIN2	0	-	0.3 V_{DD}	V
	V_{IL2}	XIN2	0	-	0.3	V
Output High Voltage	V_{OH}	V_{DD} = 2.4V, I_{OH} = - 1mA, T_A = 25°C	V_{DD} - 0.7	-	-	V
Output Low Voltage	V_{OL}	V_{DD} = 2.4V, I_{OL} = 1mA, T_A = 25°C	-	0.4	1	V
Output High Current	I_{OH}	V_{DD} = 2.4V, V_{OH} = 2.2V T_A = 25°C	-	-2	-	mA
Output Low Current	I_{OL}	V_{DD} = 2.4V, V_{OH} = 2.2V T_A = 25°C	-	2	-	mA
Input High Leakage Current	I_{LIH1}	All input pins except PROG, XIN2 and XOUT2, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	XIN2 and XOUT2, V_{IN} = V_{DD}	-	-	20	µA
	I_{LIH3}	PROG, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins except XIN2 and XOUT2, V_{IN} = 0	-	-	-1	µA
	I_{LIL2}	XIN2 and XOUT2, V_{IN} = 0	-	-	20	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	40	80	160	kΩ
Pull-down Resistors	R_{PD}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Supply Current Run Mode [1]	I_{dd}(op)	MCLK = RCOSC clock, f_{HF} = 4MHz, V_{DD} = 3.0V, T_A = 25°C	-	2.8	3.3	mA
		MCLK = XIN2 clock, f_{XIN2} = 32.768kHz, V_{DD} = 3.0V, T_A = 25°C	-	14	23	µA
		MCLK = int. low-freq. osc. clock, f_{LF} = 50kHz, V_{DD} = 3.0V, T_A = 25°C	-	15	22.5	µA
Supply Current Idle Mode [1]	I_{dd}(id)	MCLK = RCOSC clock, f_{HF} = 4MHz, V_{DD} = 3.0V, T_A = 25°C	-	1.8	2.3	mA
		MCLK = XIN2 clock, f_{XIN2} = 32.768kHz, V_{DD} = 3.0V, T_A = 25°C	-	11	18	µA
		MCLK = int. low-freq. osc. clock, f_{LF} = 50kHz, V_{DD} = 3.0V, T_A = 25°C	-	11	18	µA
Supply Current Power Down Mode [2]	I_{dd}(pd)	LCLK = XIN2 clock, f_{XIN2} = 32.768kHz, V_{DD} = 3.0V, T_A = 25°C	-	5	7.5	µA
		LCLK = int. low-freq. osc. clock, f_{LF} = 50kHz, V_{DD} = 3.0V, T_A = 25°C	-	2	5	µA
		f_{HF} = stop, f_{XIN2} = stop, f_{LF} = stop, V_{DD} = 3.0V, T_A = 25°C	-	1	2.5	µA

Remarks:
[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.
[2] Supply current is tested with all digital and analog peripherals power down, and all IO ports configured as digital input with pull-up resistor enabled.
[3] MCLK: Main system clock
LCLK: Subsystem clock
f_{HF}: Internal high-frequency oscillator clock frequency
f_{XIN2}: XIN2 clock frequency
f_{LF}: Internal low-frequency oscillator clock frequency

1.3 Low Voltage Detect circuit Characteristics

T_A = -40°C to +85°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	$\Delta V^{[1]}$		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	V_{LVD1}		1.4	1.5	1.6	V

Remarks:
[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.4 LCD Driver

T_A = -40°C to +85°C, unless specified otherwise

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal dividing resistor for LCD power supply	R_{LCD}	RSEL = 1, V_{DD} = 3.0V	-	100	-	kΩ
		RSEL = 0, V_{DD} = 3.0V	-	200	-	kΩ
COM output impedance	R_{COM}	V_{DD} = 3.0V	-	2	-	kΩ
SEG output impedance	R_{SEG}	V_{DD} = 3.0V	-	2	-	kΩ

1.5 SRAM Data Retention Voltage in Stop Mode

T_A = -40°C to +85°C, unless specified otherwise

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Stop Mode	-	-	1	uA

1.6 Input/Output Capacitance

T_A = -40°C to +85°C, V_{DD} = 0 V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

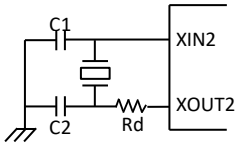
1.7 Flash Memory Data Retention

V_{DD} = 3.3V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	10k write/erase cycle, T_A = 25°C	-	50	-	Year
	t_{DRP2}	10k write/erase cycle, T_A = 85°C	-	30	-	Year
	t_{DRP3}	10k write/erase cycle, T_A = 125°C	-	5	-	Year

1.8 Oscillation Characteristics

Data are based on characterization results unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal High-Frequency RC Oscillator	f_{HF}	V_{DD} = 1.6V to 3.6V	-	4	-	MHz
Int. RC Trimmed[1] Accuracy		V_{DD} = 2V & 3.3V, T_A = 25°C	-1[2]	-	1[2]	%
		V_{DD} = 1.6V to 3.6V, T_A = 25°C	-1	-	1	%
		V_{DD} = 1.6V to 3.6V, T_A = -20°C to +85°C	-2	-	1.5	%
		V_{DD} = 1.6V to 3.6V, T_A = -40°C to +105°C	-4	-	3	%
XIN2 Clock Frequency (crystal resonator)	f_{XIN2}		-	32.768	-	kHz
Internal Low-Frequency Oscillator Clock Frequency[4]	f_{LF}	T_A = -20°C to +85°C	25	50	75	kHz

Remarks:
[1] Trimmed at T_A =25°C, V_{DD} = 3.3V
[2] Tested in production
[4] Without trimming

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal High-frequency Oscillator Stabilization Wait Time	t_{HFS}	t_{HFS} when released by internal reset	75	131	150	ms
		t_{HFS} when released by external interrupt[1]	-	$2^{11}/f_{OSC}$	-	ms
XIN2 Clock Oscillator Stabilization Wait Time	t_{XIN2S}	f_{XIN2} = 32.768kHz[2]	-	1	-	s

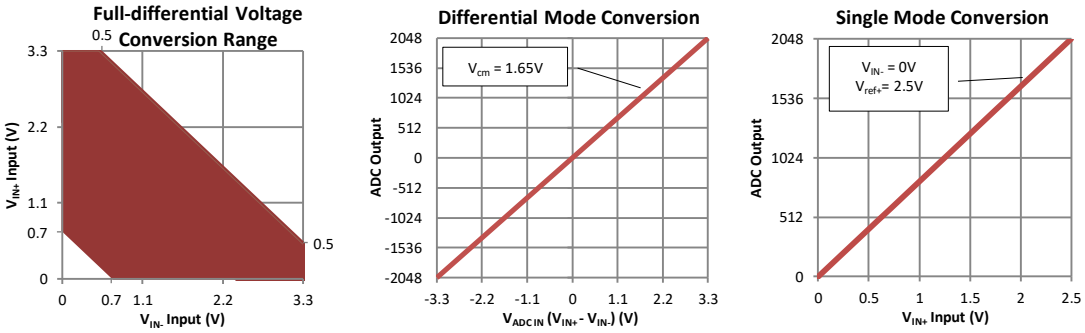
[1] The duration of the oscillation stabilization time (t_{HFS}) when it is released from power down mode by Port A or Port B interrupt.

1.9 12-bit ADC Characteristics

V_{DD} = 3.3V, $V_{ADC\ ref+}$ = 3.3V, $V_{ADC\ ref-}$ = 0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{ADC\ IN}$	-	V_{SS}	-	V_{DD}	V
Voltage Reference Range	$V_{ADC\ ref}$	-	V_{SS}	-	V_{DD}	V
ADC Voltage Resolution	-	-	1.61			mV
		External Voltage Reference	($V_{ADC\ ref+}$ +$V_{ADC\ ref-}$) /2048			
Output Resolution	-	Single-ended mode	11			bits
		Differential mode	12			
Conversion Range	-	Single-ended mode	0.7	-	V_{DD}	V
		Differential mode (V_{IN+} - V_{IN-})	- V_{DD}	-	V_{DD}	V
		Differential Common Mode Voltage* (V_{cm})	0.7	-	1.9	V
Internal Sample & Hold Capacitance	$C_{ADC\ IN}$	-	-	-	10	pF
Input Resistance	$R_{ADC\ IN}$	-	5	-	-	MΩ
Conversion Clock Frequency	f_{ADC}	V_{DD} = 2.0V – 3.3V	1	-	3.2	MHz
Sampling time	t_{ADC_S}	f_{ADC} = 3.2MHz	1			µs
		-	3			1/ f_{ADC}
Total conversion time	t_{ADC_CONV}	f_{ADC} = 3.2MHz	16			µs
		-	16			1/ f_{ADC}
Dynamic performance	ENOB	V_{DD} = 3.3V, f_{ADC} = 3MHz, T_A = 25°C	10	-	-	bits
	INL		-	1	2	LSB
	DNL		-	1	2	LSB

*Differential Common Mode Voltage = (V_{in+}+V_{in-})/2



1.10 Temperature Sensor Characteristics

V_{DD} = 3.3V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Voltage at 70°C ±2°C[1]	V_{70}	T_A = 70°C, VDD = 3.3V ± 10mV	1.1	1.3	1.5	V
Average Slope	M_{TS}		3.45	3.75	4.05	mV/°C
Start-up Time	T_{TS_Start}		-	-	10	µs
ADC Sampling Time	T_{TS_ADC}		-	20	30	µs

Remark:

1. Tested in production at VDD = 3.3V ± 10mV and store in the TEMP_V70 byte.

1.11 Bandgap Voltage Reference

V_{DD} = 3.3V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{BG}	T_A = 70°C, VDD = 3.3V ± 10mV	2.35	2.40	2.45	V
Temperature trimming in system application	V_{BGT}	Firmware trimming to 2.4V, T_A = -40°C – 105°C, VDD = 3.3V	-	2.40	-	V
Short-circuit Current	I_{OBG}		-	200	-	µA
Turn-on Time	$T_{BGReady}$		-	50	-	µs
Supply Rejection Ratio			-	20	-	mV/V

1.12 Thermal Characteristics

The maximum junction temperature (T_{JMAX}) can be calculated using the below equation:

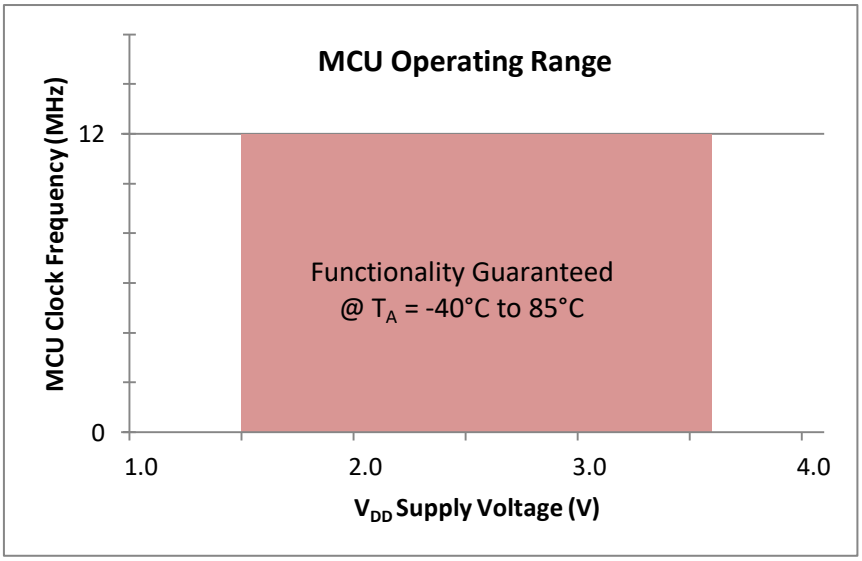
$T_{JMAX} = T_{AMAX} + (P_{DMAX} \times \theta_{JA})$

Where:

- T_{AMAX} is the maximum ambient temperature in °C
- θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{DMAX} is the sum of P_{INTMAX} and P_{IOMAX} ($P_{DMAX} = P_{INTMAX} + P_{IOMAX}$)
- P_{INTMAX} is the maximum internal power of the chip. It is calculated as the product of V_{DD} and I_{DD}, expressed in Watts.
- P_{IOMAX} is the maximum power dissipation of output pins, where
  $P_{IOMAX} = \sum (V_{OL}*I_{OL}) + \sum ((V_{DD} - V_{OH})*I_{OH})$,
  and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the IOs at low and high level of the application

Package thermal characteristics is shown in the table below are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment. More information about JESD51-2 can be found in www.jedec.org.

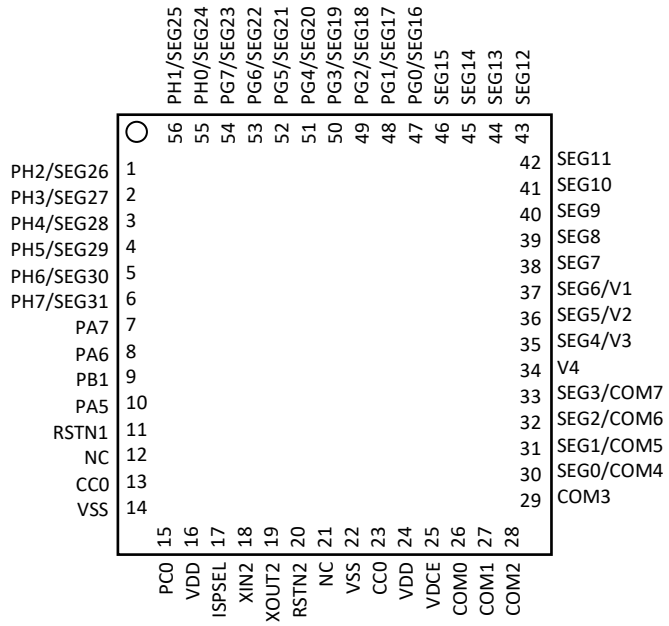
Parameter	Symbol	Parameters	Value	Unit
Maximum Junction Temperature	T_{Jmax}		+105	°C
Thermal Resistance junction-ambient	θ_{JA}	QFN56 8mm x 8mm	42	°C/W
		QFN88 10mm x 10mm	40	°C/W
		LQFP128 14mm x 14mm	35	°C/W
		QFN128 14mm x 14mm	40	°C/W



2 Pin Assignment

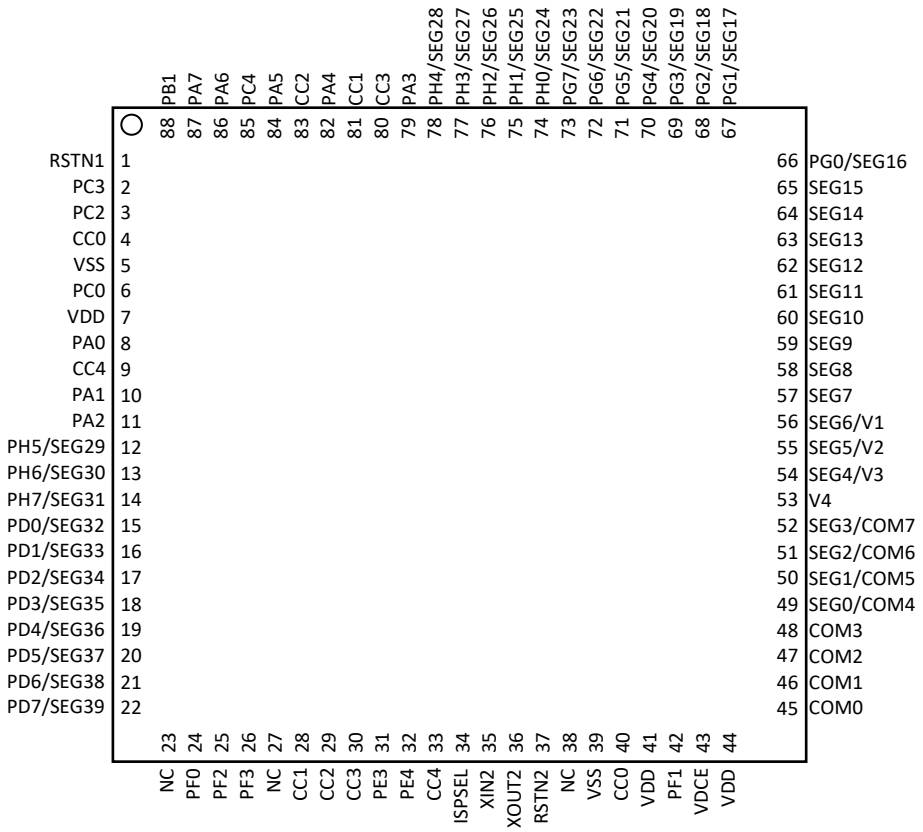
2.1 DC6288FD32Z6 – QFN56, 32 seg x 4 com / 28 seg x 8 com

(QFN56)



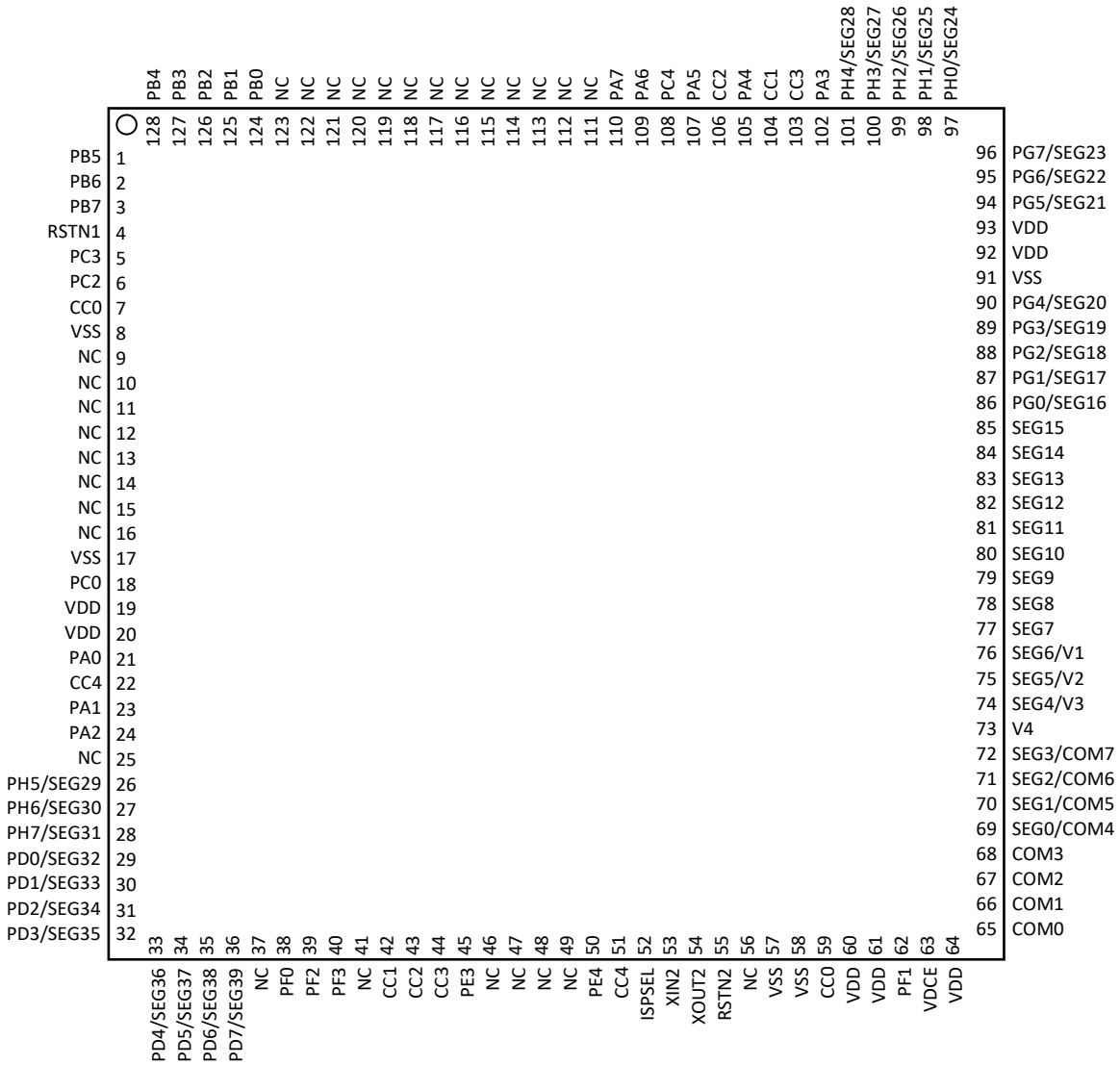
2.2 DC6288FD32V6 – QFN88, 40 seg x 4 com / 36 seg x 8 com

(QFN88)



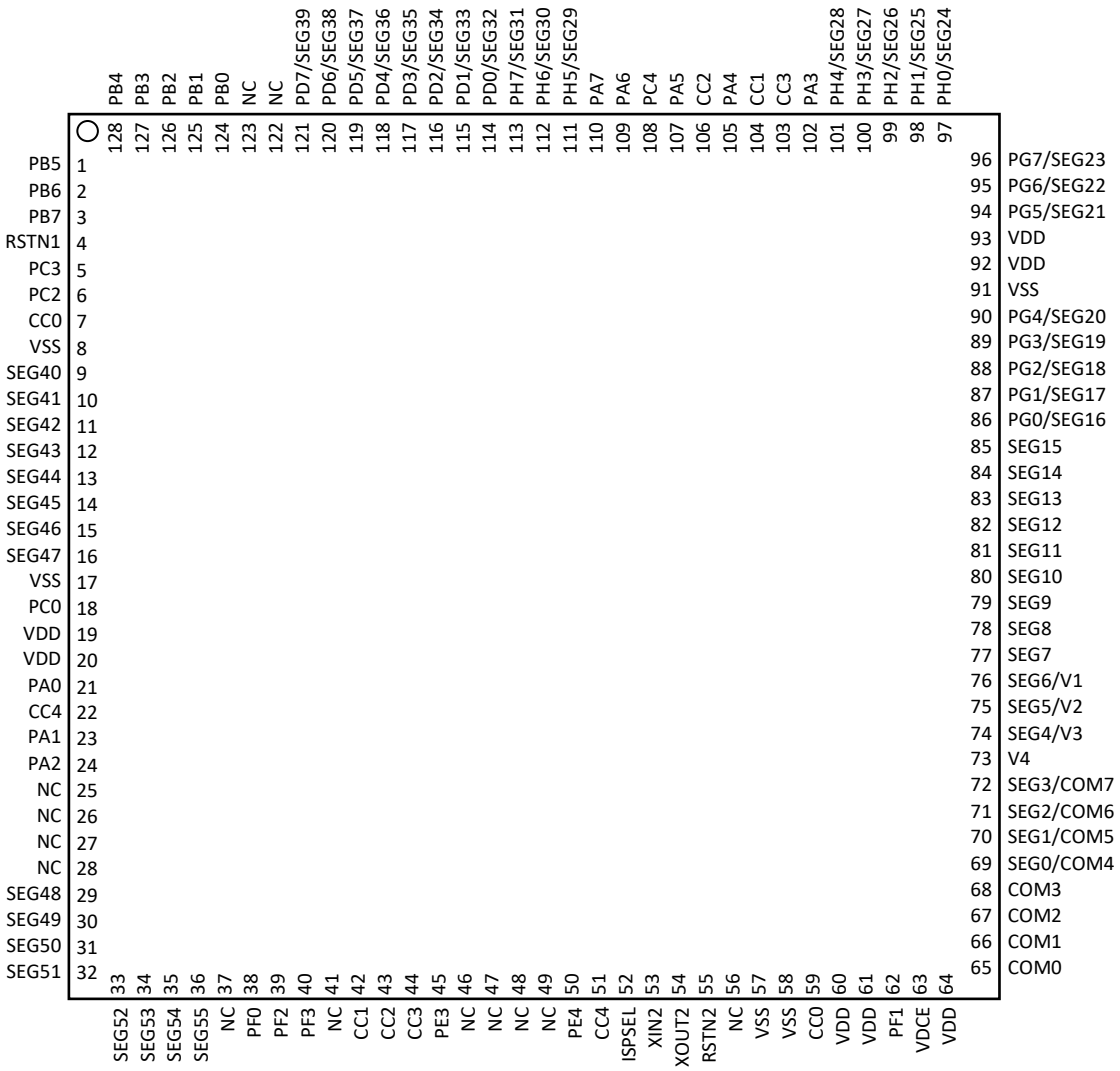
2.3 DC6288FD32B4A/B6A – LQFP128 / QFN128, 40 seg x 4 com / 36 seg x 8 com

(QFN128)



2.4 DC6288FD32B4B/B6B – LQFP128 / QFN128, 56 seg x 4 com / 52 seg x 8 com

(QFN128)



GPIO

Pin	Function	Timer / PWM	Communication	Other	Analog (Ch.1/Ch.2)
PA0	Type A GPIO w/ Interrupt	T0/T24EX/T24CC	-	-	ADC V+ / ADC V-
PA1	Type A GPIO w/ Interrupt	T2EX	SDA (I^2C)	-	ADC V+ / ADC V-
PA2	Type A GPIO w/ Interrupt	T2/T2OUT	SCK (I^2C)	CNVSTR (ADC)	ADC V+ / ADC V-
PA3	Type A GPIO w/ Interrupt	T2CC3	-	-	ADC V+ / ADC V-
PA4	Type A GPIO w/ Interrupt	T2CC4	-	MCLK	ADC V+ / ADC V-
PA5	Type A GPIO w/ Interrupt	T24OUT	SDO(SPI) / TX(UART0)*	-	ADC V+ / ADC V-
PA6	Type A GPIO w/ Interrupt	T2CC1	SDI(SPI) / RX(UART0)*	-	ADC V+ / ADC V-
PA7	Type A GPIO w/ Interrupt	T2CC2	SCK(SPI)	-	ADC V+ / ADC V-
PB0	Type A GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PB1	Type A GPIO w/ Interrupt	T1	-	SL (ISP-SL)	ADC V+ / ADC V-
PB2	Type A GPIO w/ Interrupt	-	-	-	ADC V+ / ADC VREF-
PB3	Type A GPIO w/ Interrupt	T24CB	-	-	ADC V+ / ADC V-

PB4	Type A GPIO w/ Interrupt	T24CA/PWM0	-	-	ADC V+ / ADC V-
PB5	Type A GPIO w/ Interrupt	-	TX (UART0)	-	ADC V+ / ADC V-
PB6	Type A GPIO w/ Interrupt	-	RX (UART0)	-	ADC V+ / ADC V-
PB7	Type A GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PC0	Type A GPIO w/ Interrupt	PWM1	-	-	ADC VREF+ / ADC V-
PC2-PC4	Type A GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PD0-PD7	Type B GPIO w/Interrupt	-	-	-	-
PE3-PE4	Type B GPIO w/ Interrupt	-	-	-	-
PF0-PF3	Type B GPIO w/ Interrupt	-	-	-	-
PG0-PG7	Type B GPIO w/ Interrupt	-	-	-	-
PH0-PH7	Type B GPIO w/ Interrupt	-	-	-	-

Type A GPIO: Hi-Z, or Totem Pole, or N-ch OD; Each mode w/ selectable pull-up/pull-down resistor
Type B GPIO: Hi-Z w/ selectable pull-up/pull-down resistor, or Totem Pole, or N-ch OD

Special

Pin	Function	Remarks	Other
RSTN1, RSTN2	External Reset (Active-low)	Capacity load must be <50pF	ECLK (ISP-SL)
XIN2, XOUT2	32.768kHz Crystal Resonator Input, Output	-	-
COM0 – COM7	LCD Common Output	-	-
SEG0 – SEG55	LCD Segment Output	-	-
V1 – V4	LCD Power Supply Pin (External)	-	-
VDCE	LVD Reset Enable	-	-
CC0 – CC4	Closed Connection Pins	Connect the pin pair externally via PCB.	-
NC	No Connection	-	-
ISPSEL	Programming Pin	-	-
VDD	MCU Power Supply	Require 100uF + 0.1uF decoupling capacitor	-
VSS	MCU Power Ground	-	-

3 Architecture Overview

DC6288FD is an 8-bit Microcontroller Unit (MCU) with low voltage embedded Flash memory, internal high accuracy RC oscillator, LCD driver, analogue to digital converter (ADC), digital peripherals, and more for general low power or handheld applications.

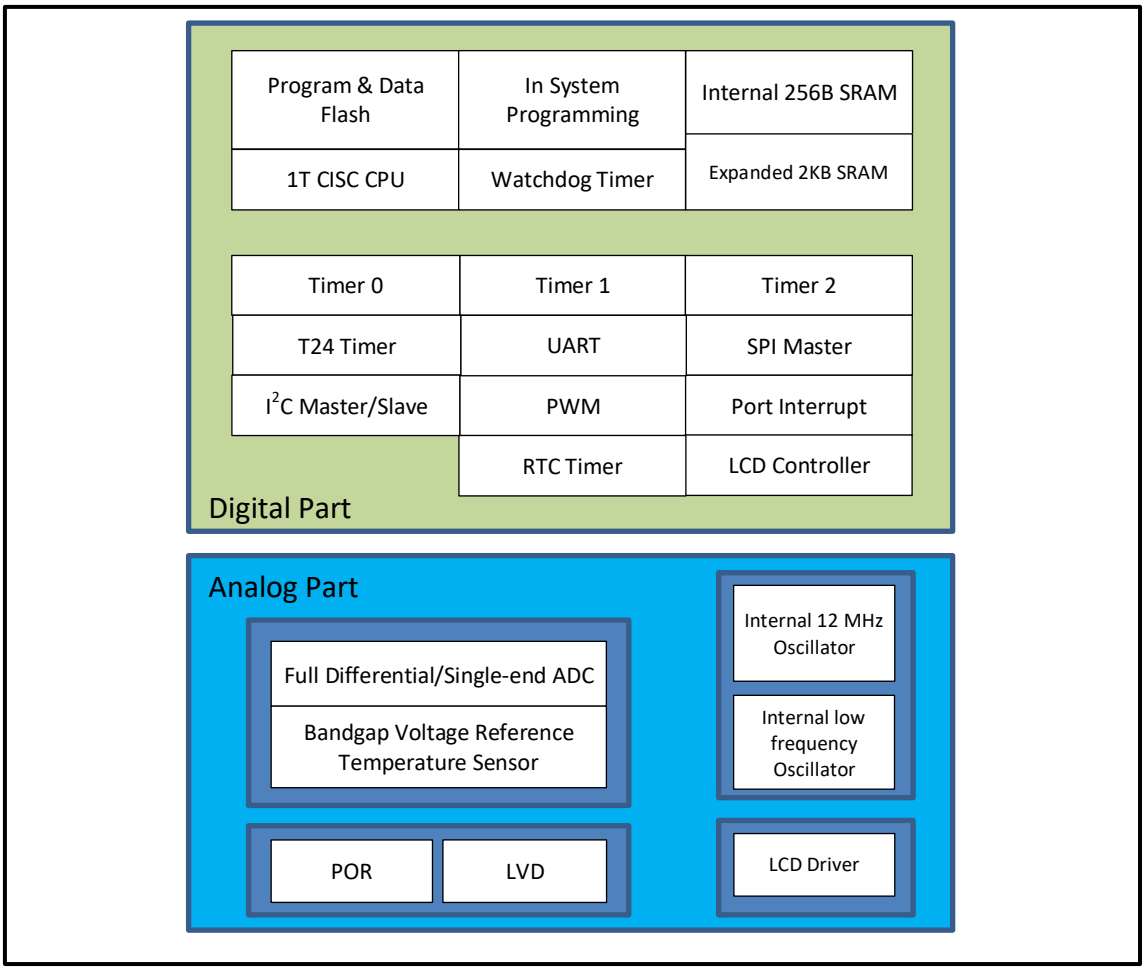
As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

The internal RC oscillator can generate clock signal without any external components, and provide an accurate system clock that is trimmed from factory or by In-system Programmer during MCU programming for a more precise clocking.

The MCU also comes with array of timers/counters that can be configured for varies timing or counting needs. There are also capable for generate pulse width modulation signals automatically, allowing system control via analogue means.

The built-in communication peripherals provide an automated support for standard protocols used for module to module communication.

The 12 bit full differential, or 11 bit single-ended, successive approximation ADC with IO channel multiplexing provides a fast, accurate, and flexible analogue to digital interface for connecting the sensors to the MCU. It supports single, continuous, timer, or external event conversion mode. It also supports window watchdog that allow user program to react to analog event automatically.



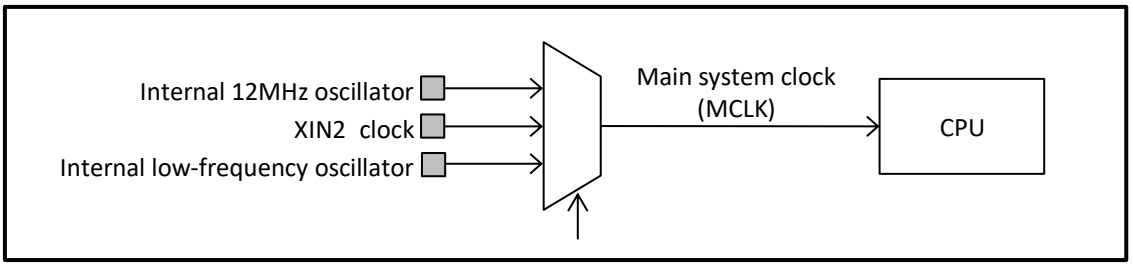
4 Central Processing Unit (CPU)

The 1T CISC CPU (Central Processing Unit) consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

Either one of the three clock sources can be supplied to CPU. For more detail clock generator diagram, refer to section 3 of the user guide.



5 Memory

Memory comprises of the following elements, namely:

- 32KB Flash memory for Code and Data usage
- 256B Internal SRAM
- 2KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

The embedded Flash memory can be partitioned for program or data memory use in 512 byte interval. It can be read and write by user program via the built-in Flash controller peripheral. In addition, the write operation is protected by write protection signature to avoid writing accidentally.

6 I/O port

There are eight GPIO ports on the MCU, Port A, B, C, D, E, F, G, and H.

The 56-pin QFN package has one 3-bit port (port A), two 1-bit ports (port B and port C), and two 8-bit ports (port G and port H).

The 88-pin QFN package has four 8-bit ports (port A, port D, port G, and port H), two 4-bit ports (port C and port F), one 2-bit port (port E), and one 1-bit port (port B).

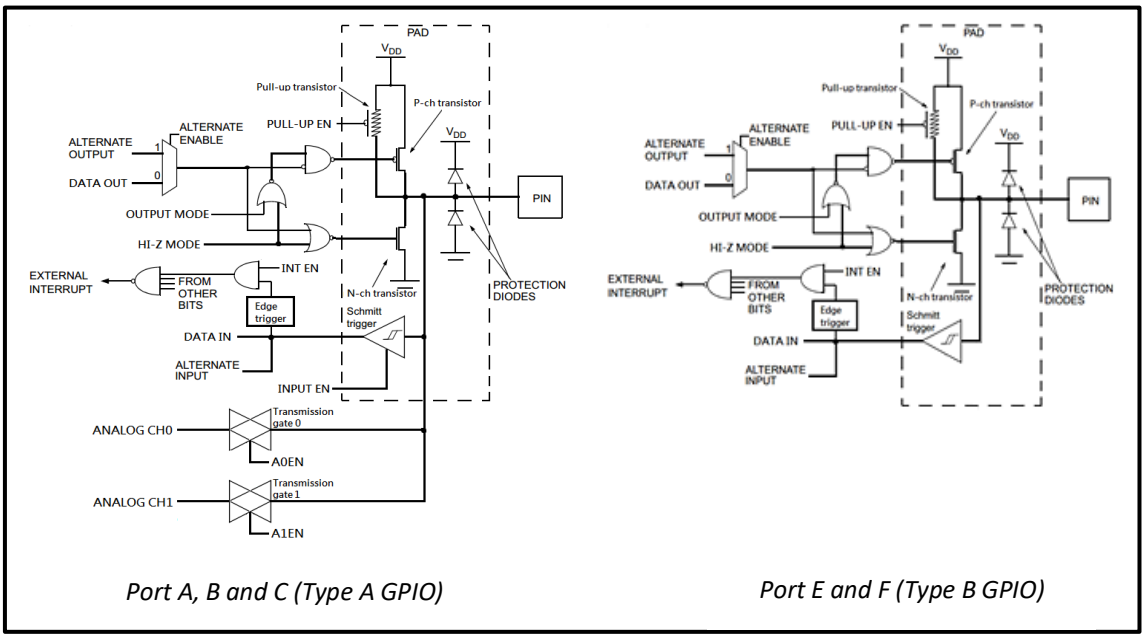
The 128-pin LQFP/QFN package has five 8-bit ports (port A, port B, port D, port G, and port H), two 4-bit ports (port C and port F), and one 2-bit port (port E). All ports are latches used to drive the bi-directional I/O lines.

Each individual pin on Port A, B and C has the following feature that can be configure independently:

- Digital output mode (High impedance, push-pull, and open-drain mode)
- Pull-up resistor
- Input Schmitt trigger
- Interrupt trigger (Rising, falling, or both edge)
- Analogue channels

Each individual pin on Port E and F has the following configuration modes:

- Digital high impedance input mode with rising edge interrupt
- Digital high impedance input mode with pull-up resistor and falling edge interrupt
- Digital bi-direction open-drain mode with both edge interrupt
- Digital push-pull output mode



Port A, B and C (Type A GPIO)

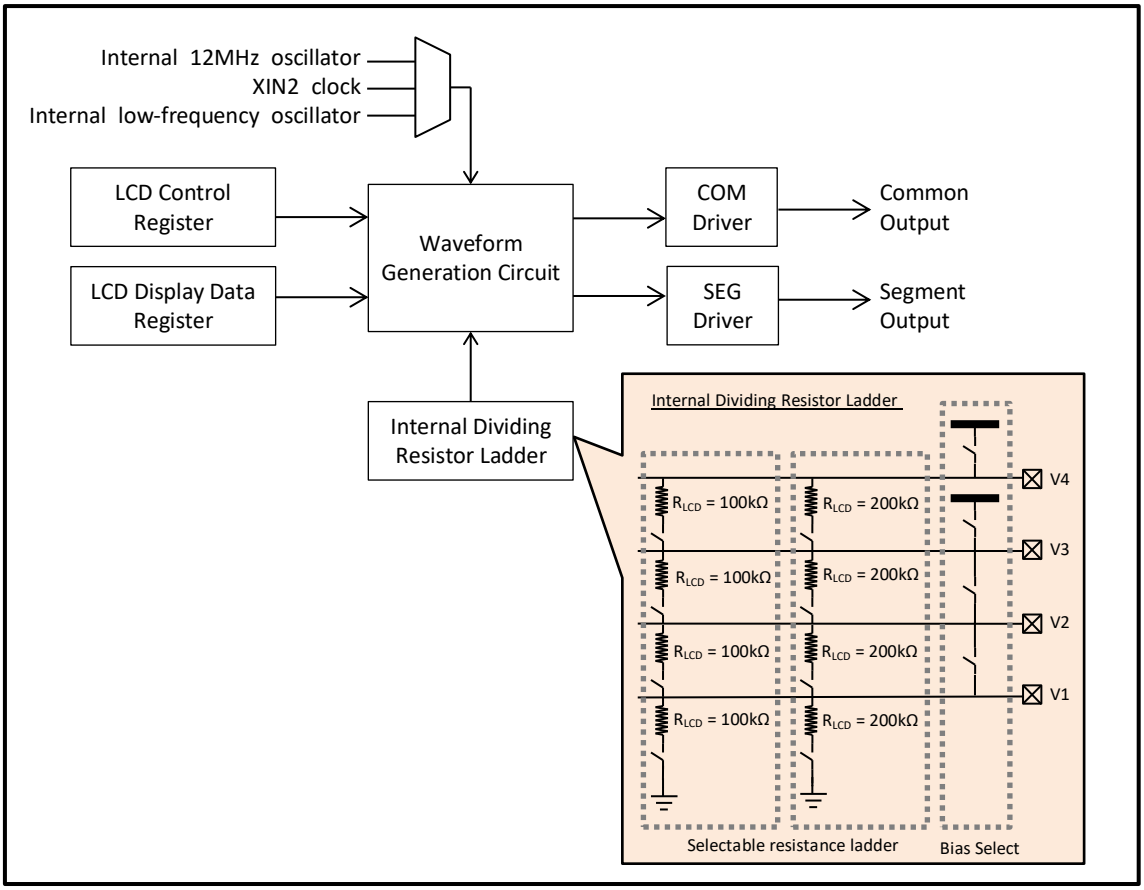
Port E and F (Type B GPIO)

7 LCD Controller / Driver

LCD controller outputs segment and common voltages to LCD display panel, according to the on-chip display memory. Display memory is stored in the internal display RAM.

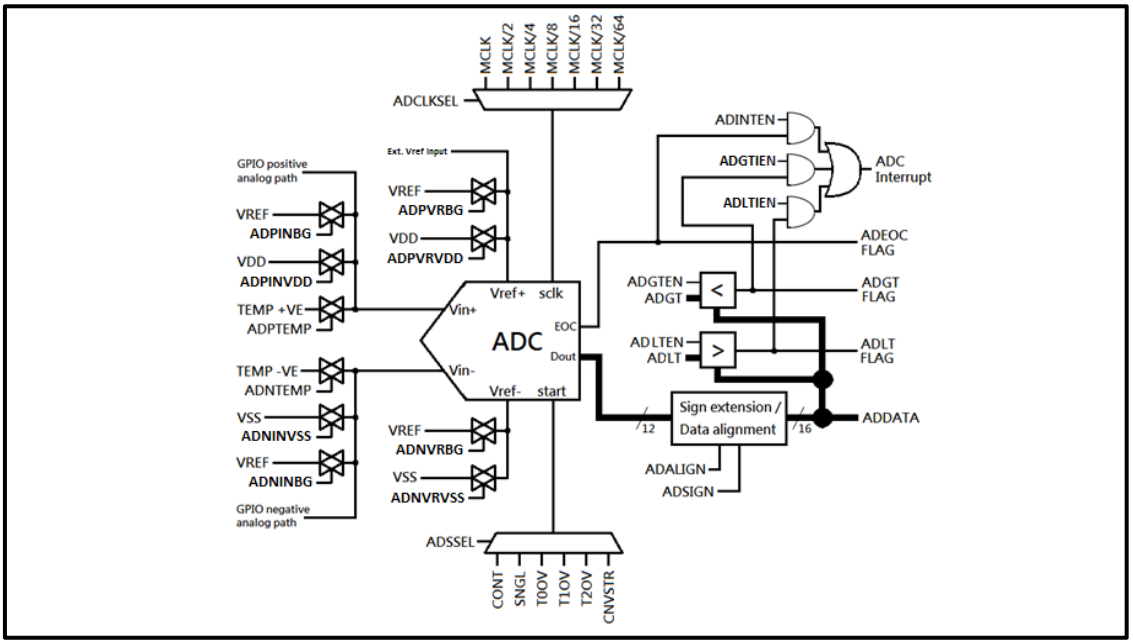
- Equip with on-chip LCD driver. Selectable resistance in 100kΩ and 200kΩ for the resistor ladder.
- Support external resistor ladder and dimming control by external variable resistor.
- 8 COM Settings
  - 1/4 bias, 1/8 duty
  - 1/3 bias, 1/8 duty
- 4 COM Settings
  - 1/2 bias, 1/2 duty
  - 1/3 bias, 1/3 duty
  - 1/3 bias, 1/4 duty
- Maximum number of displayed pixels:

Part No.	Package	Duty	Max. Display Pixels	Used COM Pins
DC6288FD32Z6	56-pin	1/2	64 pixels	COM0 – COM1
		1/3	96 pixels	COM0 – COM2
		1/4	128 pixels	COM0 – COM3
		1/8	224 pixels	COM0 – COM7
DC6288FD32V6/ DC6288FD32B4A/ DC6288FD32B6A	128-pin	1/2	80 pixels	COM0 – COM1
		1/3	120 pixels	COM0 – COM2
		1/4	160 pixels	COM0 – COM3
		1/8	288 pixels	COM0 – COM7
DC6288FD32B4B/ DC6288FD32B6B	128-pin	1/2	112 pixels	COM0 – COM1
		1/3	168 pixels	COM0 – COM2
		1/4	224 pixels	COM0 – COM3
		1/8	416 pixels	COM0 – COM7


Internal 12MHz oscillator
XIN2 clock
Internal low-frequency oscillator
LCD Control Register
LCD Display Data Register
Waveform Generation Circuit
COM Driver
SEG Driver
Common Output
Segment Output
Internal Dividing Resistor Ladder
Internal Dividing Resistor Ladder
RLCD = 100kΩ
RLCD = 200kΩ
V4
V3
V2
V1
Selectable resistance ladder
Bias Select

8 12-Bit Full-differential ADC with Single-End Input Mode

The ADC module consists of two input paths, V+ and V-, to digitize full differential signal at maximum conversion rate of 200ksps. It can also be configured to measure signal-end input. The start of conversion can be triggered by register, timer overflow or external rising-edge. The reference voltage (VREF) is also selectable from either internal, external or VDD by software configurations.



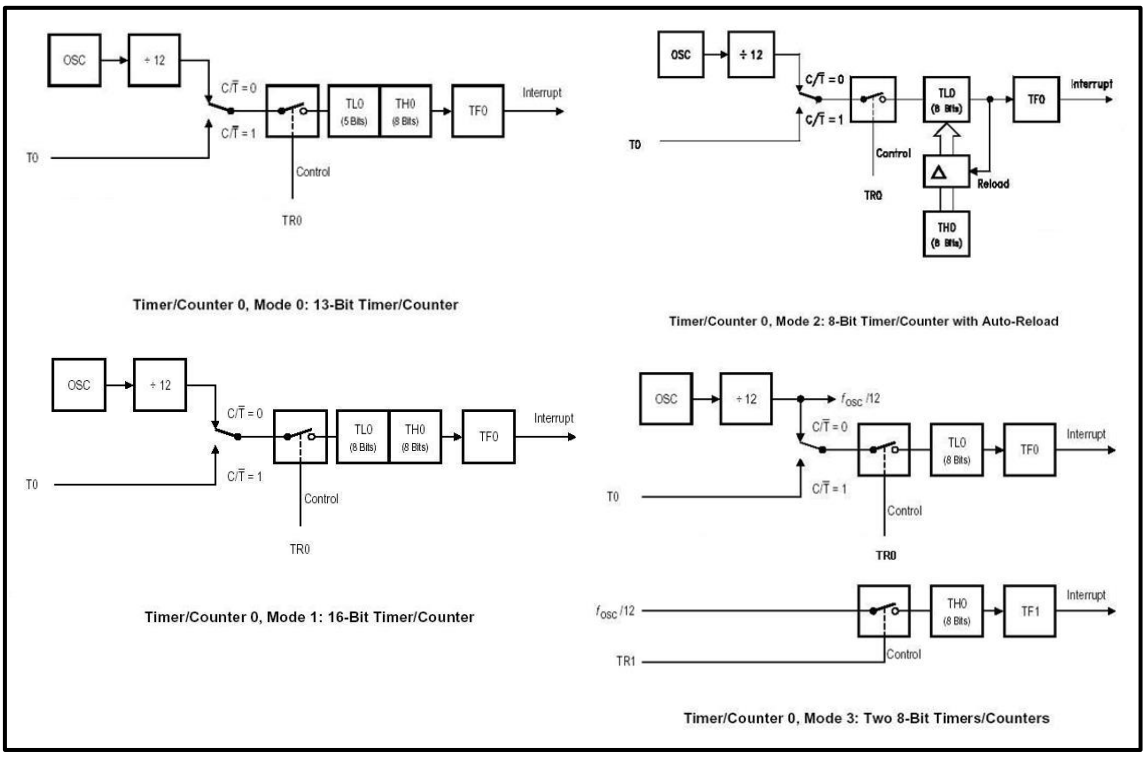
9 Internal Bandgap Voltage Reference & Temperature Sensor

The internal bandgap voltage reference can provide a fix voltage which can be used for voltage comparison and measurement. The internal temperature sensor uses the ADC to sense the on-chip temperature without external component.

10 General Purpose Timers/Counters 0 & 1

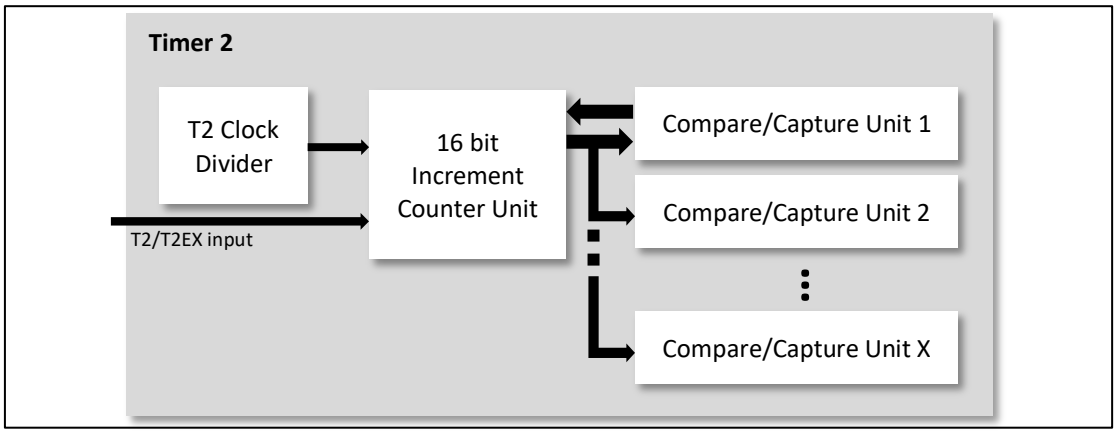
Three independent general purpose 16-bit timers/counters, Timer0, and Timer1 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.



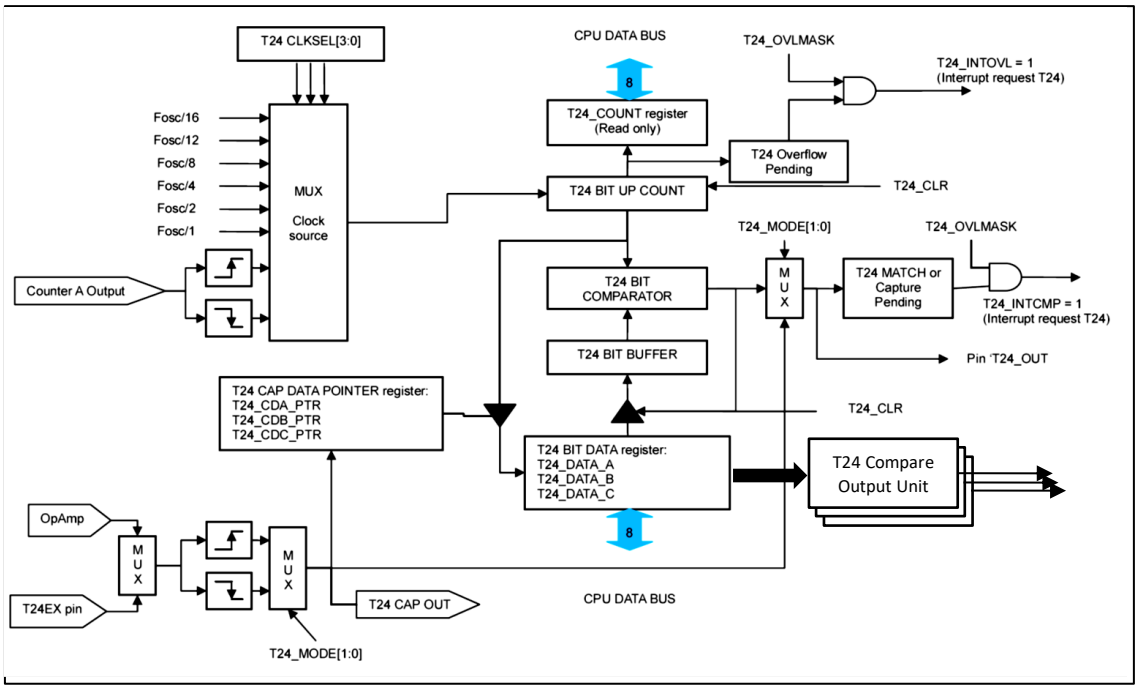
11 Timer 2

Timer 2 consists of a 16-bit timer/counter unit and multiples of compare/capture units. The timer unit itself is capable as a 16-bit system timer/counter, or an external event timer/counter. It also provides the base counter value to the compare/capture units, where each compare/capture unit can act as a system clock timer, external event timer, or PWM output generator.



12 Timer 24

Timer 24 is a 24 bit timer that provides high resolution and counting length designed to capture Infra-red signal carrier frequency as high as 500kHz for event 2 seconds apart. In capture mode, there is 3 capture registers that can time 3 events automatically without servicing. It can also operate as interval timer mode and compare mode which can generates interrupt for timing purposes, and/or pulse width modulation (PWM) outputs.



13 Enhanced UART

The UART controller is fully compatible with the standard serial channel with enhancement. The UART perform framing error detection and automatic address recognition in all four modes (one synchronous and three asynchronous. It supports multiprocessor communication as does the standard UART protocol.

14 Inter-Integrated Circuit (I^2C) Interface

The I^2C Bus Controller supports all transfer modes from and to the I^2C bus and transfers up to 100kbit/s in the standard mode or up to 400kbit/s in the fast mode. The I^2C logic handles bytes transfer autonomously which keeps track of serial transfers, with status registers reflect the status of the I^2C Bus Controller and the I^2C bus to applications. The interface also supports the System Management Bus (SMBus) protocol where additional timeout detection is added.

15 Serial Peripheral Interface

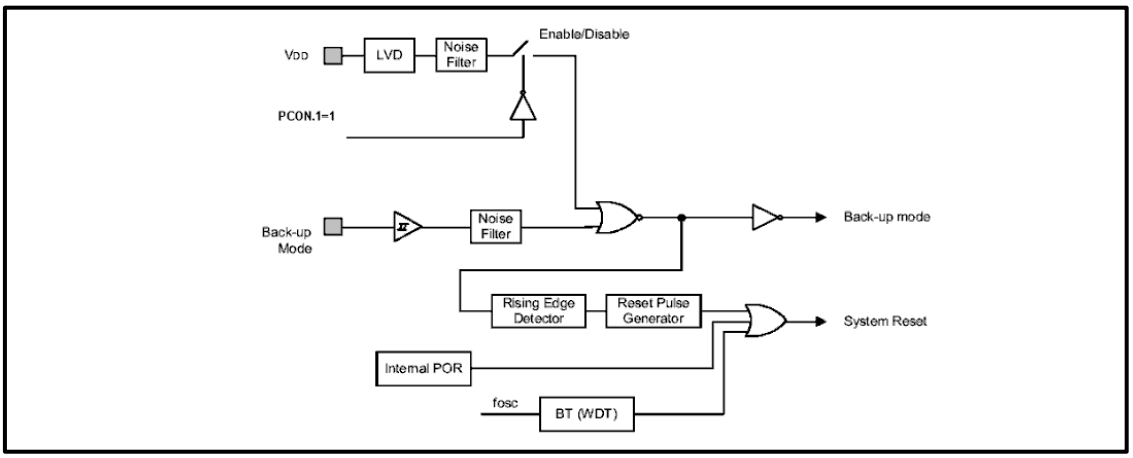
The integrated master mode Serial Peripheral Interface (SPI) controller allows data to be synchronously transmitted and received simultaneously with bit rate up to 4Mbits/s between multiple external peripherals.

16 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



17 In System Programming

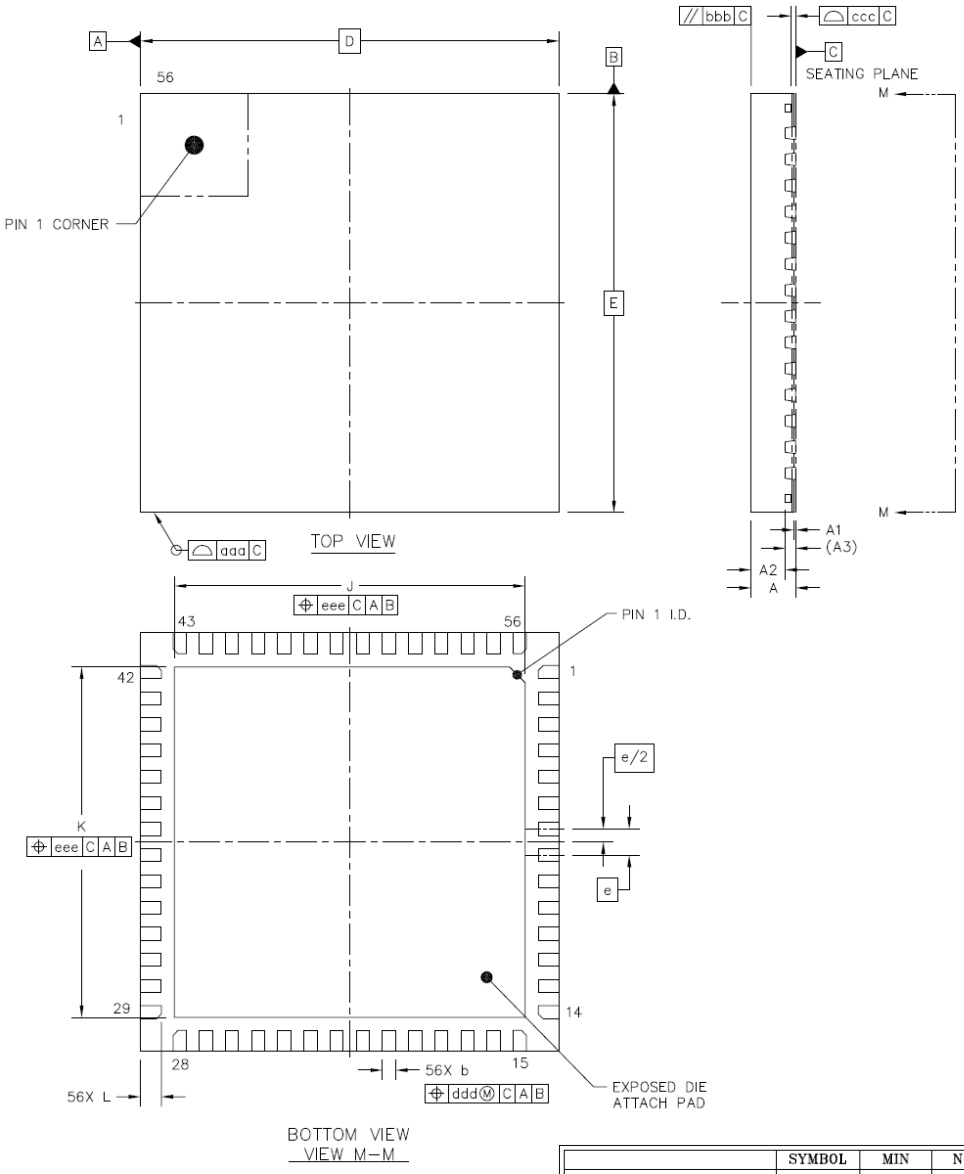
The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. The DC6288FD series support ISP-SL protocol which requires only a 2 wire bus to perform the ISP function, minimize the impact on application design.

18 Ordering Information

Part No	Package	Lead Pitch	Program Flash	SRAM	Maximum LCD segments
DC6288FD32Z6	QFN56	0.5mm	32KB Configurable (Program + Data)	256B + 2KB	32 x 4 = 128 / 28 x 8 = 224
DC6288FD32V6	QFN88	0.4mm	32KB Configurable (Program + Data)	256B + 2KB	40 x 4 = 160 / 36 x 8 = 288
DC6288FD32B4A	LQFP128	0.4mm	32KB Configurable (Program + Data)	256B + 2KB	40 x 4 = 160 / 36 x 8 = 288
DC6288FD32B4B	LQFP128	0.4mm	32KB Configurable (Program + Data)	256B + 2KB	56 x 4 = 224 / 52 x 8 = 416
DC6288FD32B6A	QFN128	0.4mm	32KB Configurable (Program + Data)	256B + 2KB	40 x 4 = 160 / 36 x 8 = 288
DC6288FD32B6B	QFN128	0.4mm	32KB Configurable (Program + Data)	256B + 2KB	56 x 4 = 224 / 52 x 8 = 416

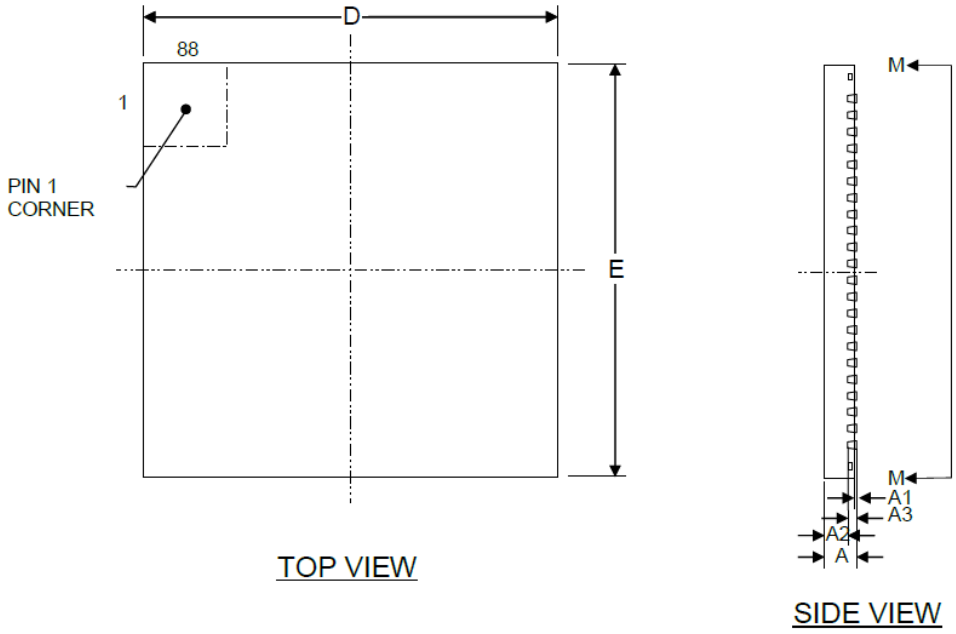
19 Package Outlines

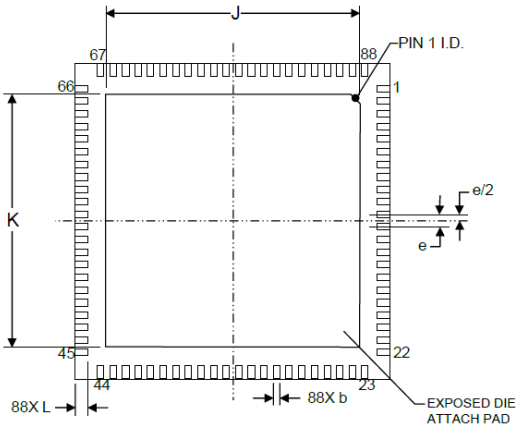
19.1 56-pin QFN



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	6.6	6.7	6.8
	Y	K	6.6	6.7	6.8
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

19.2 88-pin QFN

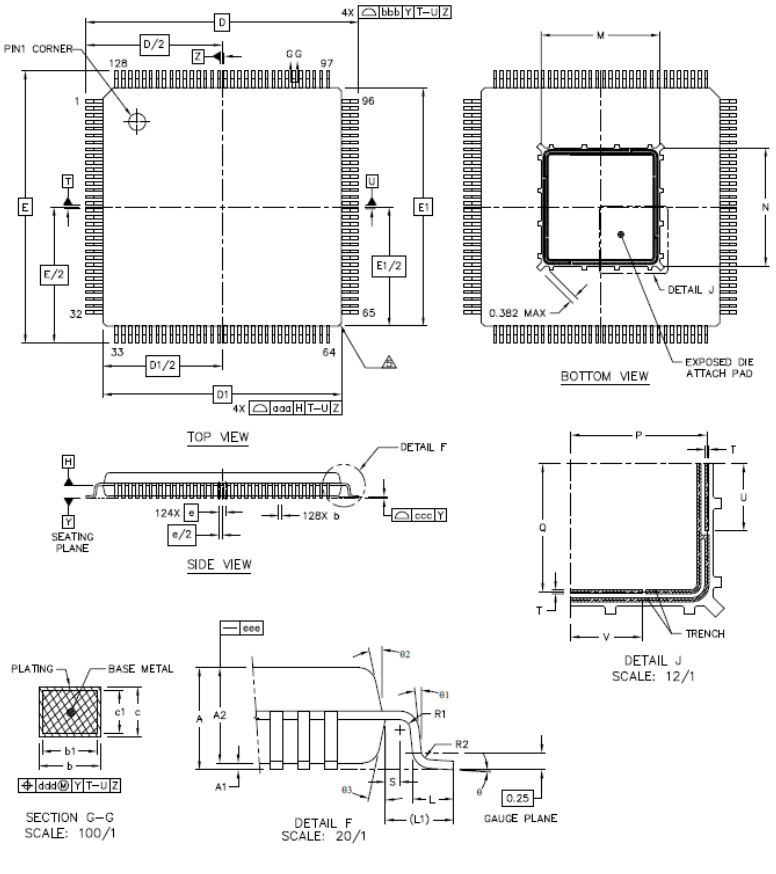




BOTTOM VIEW
VIEW M－M

Symbols	Dimension in mm[27]			Dimension in inch		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.80	0.90	0.028	0.031	0.035
A1	0.00	0.035	0.05	0	0.001	0.002
A2	NA	0.55	0.57	NA	0.022	0.022
A3		0.203 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D		10.00 BSC			0.394 BSC	
E		10.00 BSC			0.394 BSC	
e		0.40 BSC			0.016 BSC	
J	6.50	7.50	8.50	0.256	0.295	0.335
K	6.50	7.50	8.50	0.256	0.295	0.335
L	0.30	0.40	0.50	0.012	0.016	0.020

19.3 128-pin LQFP



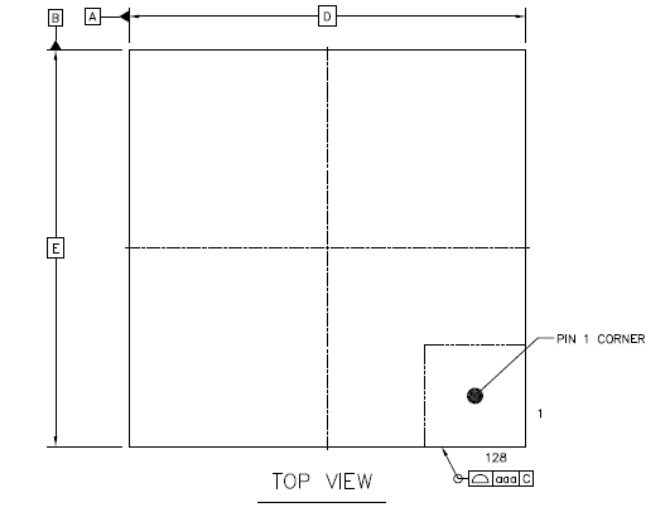
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
LEAD THICKNESS(PLATING)		c	0.09	---	0.2
LEAD THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D		16 BSC	
	Y	E		16 BSC	
	X	D1		14 BSC	
	Y	E1		14 BSC	
EXPOSED PAD SIZE	X	M	6.855	6.955	7.055
	Y	N	6.855	6.955	7.055
LEAD PITCH		e		0.4 BSC	
		L	0.45	0.6	0.75
FOOTPRINT		L1		1 REF	
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
		P	3.278	3.328	3.378
		Q	3.078	3.128	3.178
		T	0.05	---	0.15
		V	1.639	---	1.839
		U	1.539	---	1.739
PACKAGE EDGE TOLERANCE		aaa		0.2	
LEAD EDGE TOLERANCE		bbb		0.2	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.07	
MOLD FLATNESS		eee		0.05	

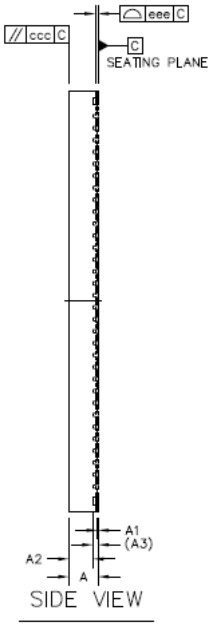
NOTES

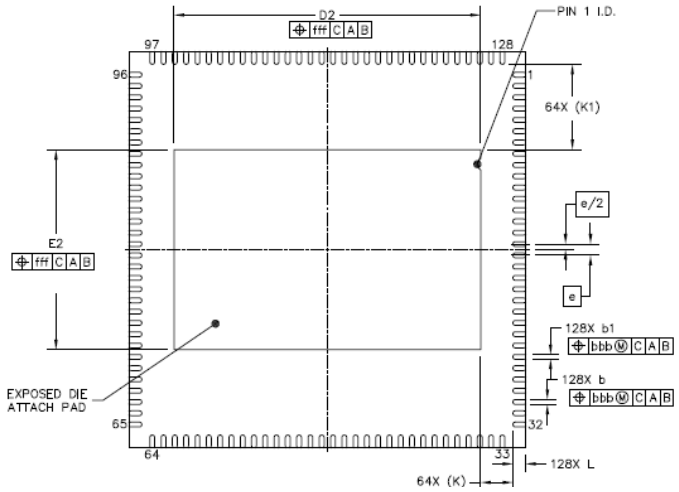
1. DATUM T, U, AND Z TO BE DETERMINED AT DATUM PLANE H.
2. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE DATUM Y.
3. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS D1 AND E1 DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE DATUM H.
4. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08 mm. DAM BAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD IS 0.07 mm.

⚠ EXACT SHAPE OF EACH CORNER IS OPTIONAL.

19.4 128-pin QFN







		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.7	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.1	0.15	0.2
		b1	0.1	0.13	---
BODY SIZE	X	D		14 BSC	
	Y	E		14 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	9.4	9.5	9.6
	Y	E2	6.1	6.2	6.3
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		1 REF	
		K1		2.65 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

20 **Revision History**

Document Rev No.	Issued Date	Section	Page	Description	Editor	Reviewer
0.6	May, 2016	-	-	Update to latest design	Patrick Li	-
0.72	Aug, 2017	-	-	Combined DC6288FT8/16/32	Patrick Chan	-
0.9	Feb 2018	-	-	Added QFN20 & QFN24 pin assignment Changed 16MHz to 12MHz	Patrick Chan	-
1.0	Mar 2018	-	-	Changed 6688FTxY6 to 6288FtxY6	Patrick Chan	-
1.1	Mar 2018	-	-	Updated QFN24 pin assignment	Patrick Chan	-
1.2	Jun 2018	-	-	Updated ADC specification	Patrick Li	-
1.3	Dec 2018	-	-	Added QFN28 pin assignment	Patrick Chan	-
1.4	May 2019	-	-	Added TSSOP20(L) pin assignment	Patrick Chan	Danny Ho
1.5	May 2019	-	-	Added thermal resistance	Patrick Chan	-
1.6	Aug 2019	-	-	Revised package thermal resistance Added TSSOP24 pin assignment	Patrick Chan	-
1.7	Mar 2020	-	-	Updated TSSOP24 pin 1-5 Updated Oscillator stabilization wait time Updated temperature sensor & bandgap	Patrick Chan, Patrick Li	Danny Ho
1.8	Mar 2020	-	-	Update pin function and GPIO	Patrick Li	-
1.9	Apr 2020			Added SOP8 pin assignment	Patrick Chan	-
2.0	Jun 2020	1.6	-	Update data retention	Danny Ho	-
2.1	Jul 2020	1.10	-	Update Bandgap Specification	Patrick Li	-
2.2	Jan, 2021	1.9	-	Update Temperature Sensor Specification	Danny Ho	-
		1.10	-	Update Bandgap Specification	-	-
1.0	Sep, 2021	All	All	Updated all LCD-related sections and released as 6288FD32 series	Patrick Chan	-
1.1	Sep, 2021	2, 6, 7, 18, 19.1	-	Added DC6288FD32Z6 QFN56 package support Added general-purpose I/O (port D, G, and H) which are mux'ed with SEG pins.	Patrick Chan	-
1.2	Nov, 2021	2,18,19	-	Updated pin assignment of all products Updated from LQFP128 to QFN128 package Updated Package Outline of QFN128 Updated Ordering Info from B4A/B to B6A/B	Patrick Chan	-
1.3	Dec, 2021	2, 18, 19	-	Added LQFP128 package support Modified QFN128 Package Outline	Patrick Chan	-
1.31	Dec, 2021	2, 18, 19	-	Modified QFN128 Package Outline Added QFN88 package support	Patrick Chan	-

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