DC6288FT

Mixed-Signal Flash Microcontroller

DC6288FT is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and digital and analog peripherals suitable for mixed-signal application. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- CPU
  - High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Memory
  - 8KB/16KB/32KB Configurable Program & Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 1KB/1.5KB/2KB SRAM
- Clock
  - Internal 12MHz oscillator with ± 1% accuracy from -20°C to +70°C, V_{DD} = 1.8V to 3.6V
  - Internal low power low frequency oscillator
- I/O Ports, Timers, Counters, & PWM
  - General Purpose I/O ports x 13/17/21/25
  - 16-bit Timers x 2
  - 16-bit Timer with 4 compare/capture modules
  - 24-bit Timer with 3 compare modules
  - 16-bit Watchdog Timer x 1
  - 8-bit Pulse width modulator x 2
- Power Management
  - Power Down and Backup modes
  - Low Voltage Detection (LVD) for backup mode
  - Low Voltage Indication (LVI) - Programmable
- 12-Bit Full-differential (11bit Single-end) A/D Convertor
  - Maximum 200k samples per second
  - Internal or external start of conversion sources
  - 13/17/21 Analog channels
- Digital Peripherals
  - Integrated Enhanced UART, SPI, I^2C bus controller
- AC/DC Characteristics
  - 1.5V to 3.6V operating voltage range, -40°C to +85°C operating temperature
- Package type:
  - 20-pin TSSOP (3 pin layouts)
  - 24-pin TSSOP
  - 20-pin QFN
  - 24-pin QFN
  - 28-pin QFN

Quick look on Ordering Information

Table of Contents

1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B and C[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B and C[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Junction Temperature Range	T_J	-	-40 to +105	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:

[1] It is measured for any one of I/O pin when configured to push-pull output high.

[2] It is measured as total for Ports A, B and C when configured to push-pull output high.

[3] It is measured for any one of I/O pin when configured to push-pull output low.

[4] It is measured as total for Ports A, B and C when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL}	All input pins	0	-	0.3 V_{DD}	V
Output High Voltage	V_{OH}	V_{DD} = 2.4V, I_{OH} = - 1mA, T_A = 25°C	V_{DD} - 0.7	-	-	V
Output Low Voltage	V_{OL}	V_{DD} = 2.4V, I_{OL} = 1mA, T_A = 25°C	-	0.4	1	V
Output High Current	I_{OH}	V_{DD} = 2.4V, V_{OH} = 2.2V T_A = 25°C	-	-2	-	mA
Output Low Current	I_{OL}	V_{DD} = 2.4V, V_{OH} = 2.2V T_A = 25°C	-	2	-	mA
Input High Leakage Current	I_{LIH1}	All input pins except PROG, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	PROG, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL}	All input pins, V_{IN} = 0	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	40	80	160	kΩ
Pull-down Resistors	R_{PD}	V_{DD} = 2.4V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Supply Current Run Mode [1]	I_{dd}(op)	f_{OSC} = 12MHz, V_{DD} = 3.3V, T_A = 25°C	-	10	12	mA
Supply Current Power Down Mode [2]	I_{dd}(pd)	V_{DD} = 3.3V, T_A = 25°C	-	4	10	µA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested with all digital and analog peripherals power down, and all IO ports configured as digital input with pull-up resistor enabled.

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	V_{LVD1}		1.4	1.5	1.6	V

Remarks:

[1] $V_{LVD2} – V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage in Stop Mode

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Stop Mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 Oscillation Characteristics

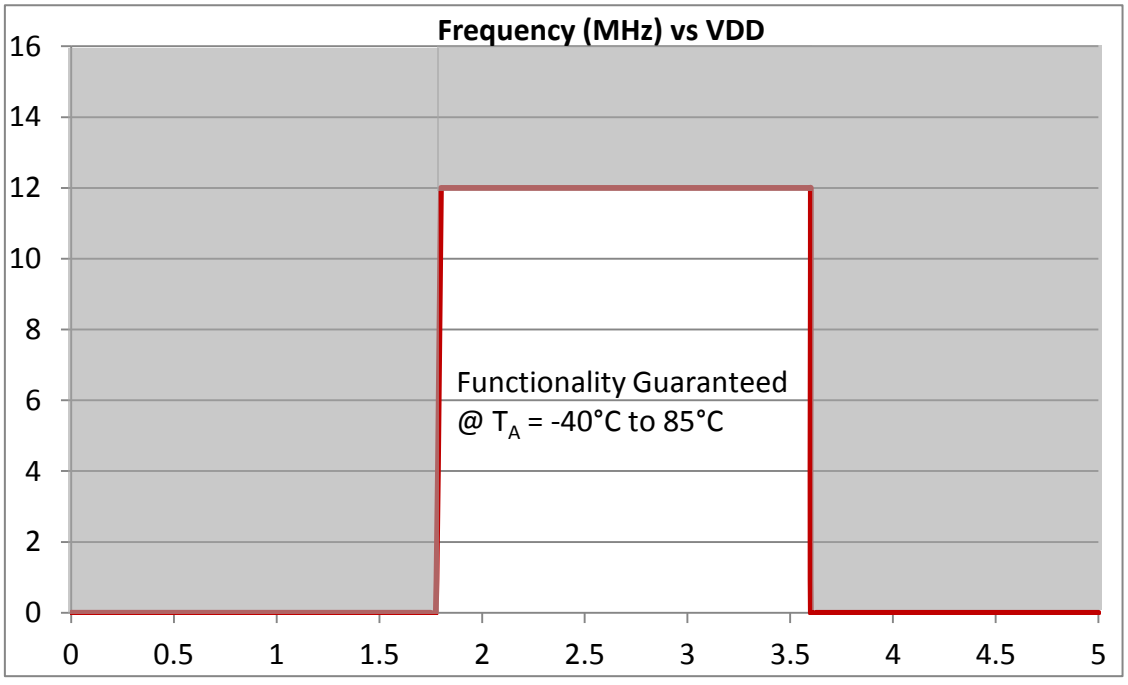
(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator		T_A = -20°C to +70°C, V_{DD} = 1.8V to 3.6V	-	-	± 1%	MHz
Oscillator Stabilization Wait Time	t_{WAIT}	t_{WAIT} when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
		t_{WAIT} when released by external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

Remarks:

[1] f_{osc} is the oscillator frequency.

[2] The duration of the oscillation stabilization time(t_{WAIT}) when it is released from power down mode by Port A or Port B interrupt.

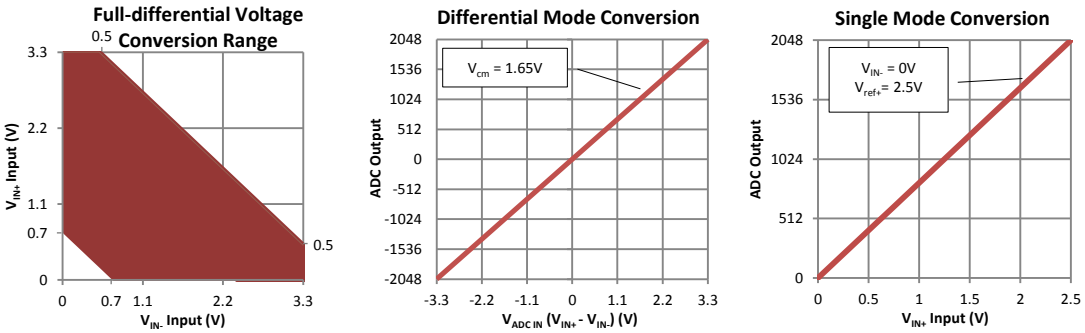


1.8 12 bits ADC Characteristics

V_{DD} = 3.3V, $V_{ADC\ ref+}$ = 3.3V, $V_{ADC\ ref-}$ = 0V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{ADC\ IN}$	-	V_{SS}	-	V_{DD}	V
Voltage Reference Range	$V_{ADC\ ref}$	-	V_{SS}	-	V_{DD}	V
ADC Voltage Resolution	-	-	1.61			mV
		External Voltage Reference	($V_{ADC\ ref+}$ +$V_{ADC\ ref-}$) /2048			
Output Resolution	-	Single-ended mode	11			bits
		Differential mode	12			
Conversion Range	-	Single-ended mode	0.7	-	V_{DD}	V
		Differential mode (V_{IN+} - V_{IN-})	- V_{DD}	-	V_{DD}	V
		Differential Common Mode Voltage* (V_{cm})	0.7	-	1.9	V
Internal Sample & Hold Capacitance	$C_{ADC\ IN}$	-	-	-	10	pF
Input Resistance	$R_{ADC\ IN}$	-	5	-	-	MΩ
Conversion Clock Frequency	f_{ADC}	V_{DD} = 2.0V – 3.3V	1	-	3.2	MHz
Sampling time	t_{ADC_S}	f_{ADC} = 3.2MHz	1			µs
		-	3			1/ f_{ADC}
Total conversion time	t_{ADC_CONV}	f_{ADC} = 3.2MHz	16			µs
		-	16			1/ f_{ADC}
Dynamic performance	ENOB	V_{DD} = 3.3V, f_{ADC} = 3MHz, T_A = 25°C	10	-	-	bits
	INL		-	1	2	LSB
	DNL		-	1	2	LSB

*Differential Common Mode Voltage = (V_{in+}+V_{in-})/2



1.9 Temperature Sensor Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Linearity			-	±0.1	-	°C
Gain			-	2.85	-	Digit/°C
Offset			-	$670_{(Dec)}$	-	Digit

1.10 Bandgap Voltage Reference

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Voltage	V_{BG}		-	1.4	-	V
Short-circuit Current	I_{OBG}		-	2	-	mA
Load Regulation		Load = 0 - 200µA to V_{SS}	-	6	-	µV/µA
Turn-on Time	$T_{BGReady}$		-	50	-	µs
Supply Rejection Ratio			-	1.1	-	mV/V

1.11 Thermal Characteristics

The maximum junction temperature (T_{JMAX}) can be calculated using the below equation:

$T_{JMAX} = T_{AMAX} + (P_{DMAX} \times \theta_{JA})$

Where:

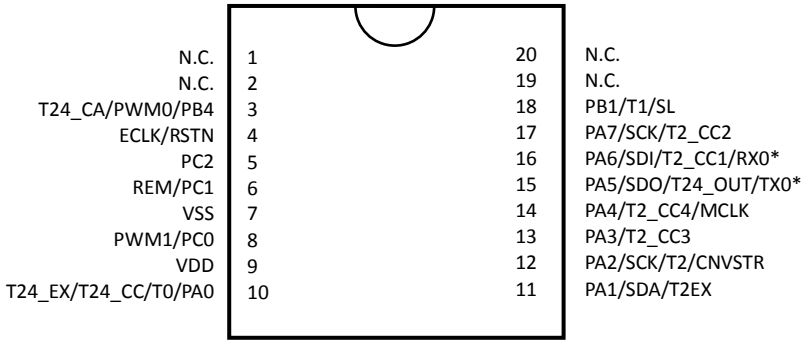
- T_{AMAX} is the maximum ambient temperature in °C
- θ_{JA} is the package junction-to-ambient thermal resistance in °C/W
- P_{DMAX} is the sum of P_{INTMAX} and P_{IOMAX} ($P_{DMAX} = P_{INTMAX} + P_{IOMAX}$)
- P_{INTMAX} is the maximum internal power of the chip. It is calculated as the product of V_{DD} and I_{DD}, expressed in Watts.
- P_{IOMAX} is the maximum power dissipation of output pins, where
  $P_{IOMAX} = \sum (V_{OL}*I_{OL}) + \sum ((V_{DD} - V_{OH})*I_{OH})$,
  and taking account of the actual V_{OL}/I_{OL} and V_{OH}/I_{OH} of the IOs at low and high level of the application

Package thermal characteristics is shown in the table below are based on JEDEC JESD51-2 with 4-layer PCB in a natural convection environment. More information about JESD51-2 can be found in www.jedec.org.

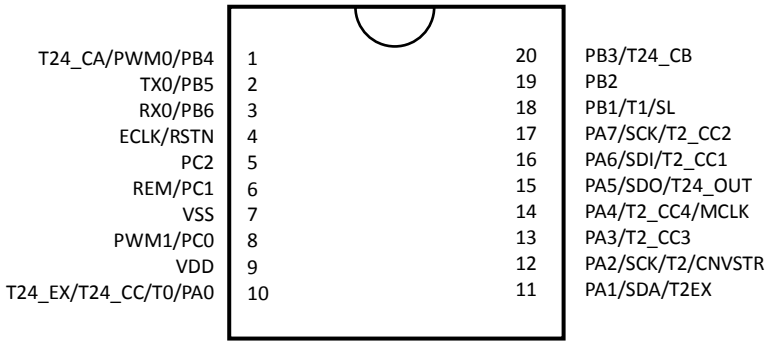
Parameter	Symbol	Parameters	Value	Unit
Maximum Junction Temperature	T_{Jmax}		+105	°C
Thermal Resistance junction-ambient	θ_{JA}	TSSOP20 6.5mm x 6.4mm	50	°C/W
		QFN20 4mm x 4mm	40	
		QFN24 4mm x 4mm	40	
		QFN28 4mm x 4mm	40	

2 Pin Assignment

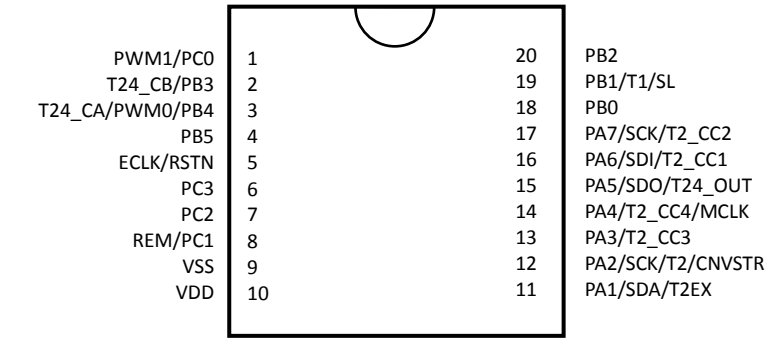
(TSSOP20 – L)



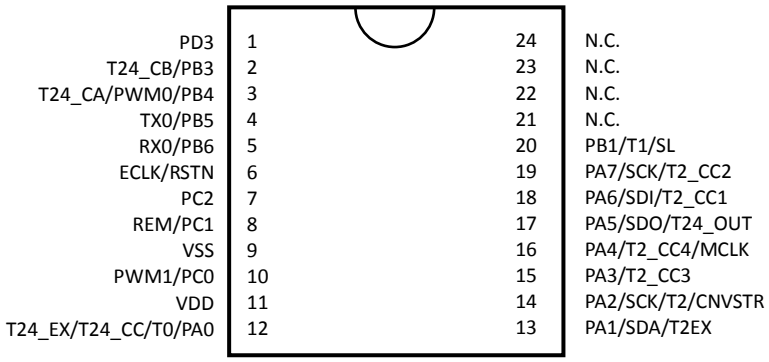
(TSSOP20 – M)



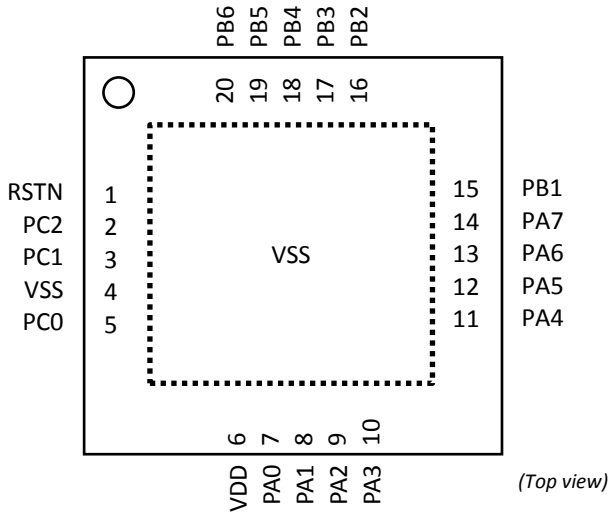
(TSSOP20 – R)



(TSSOP24 - L)

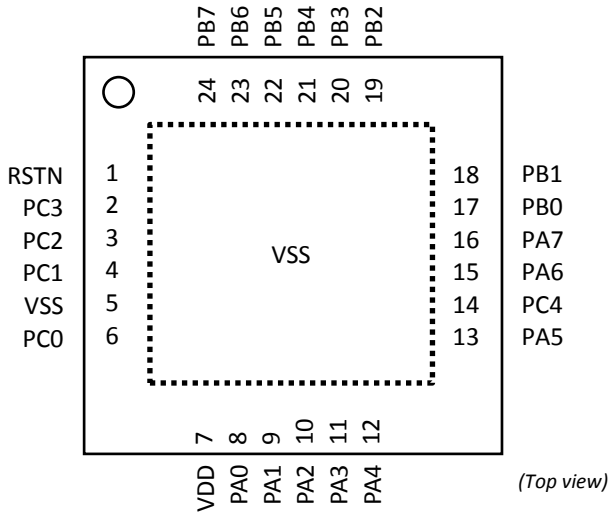


(QFN20)



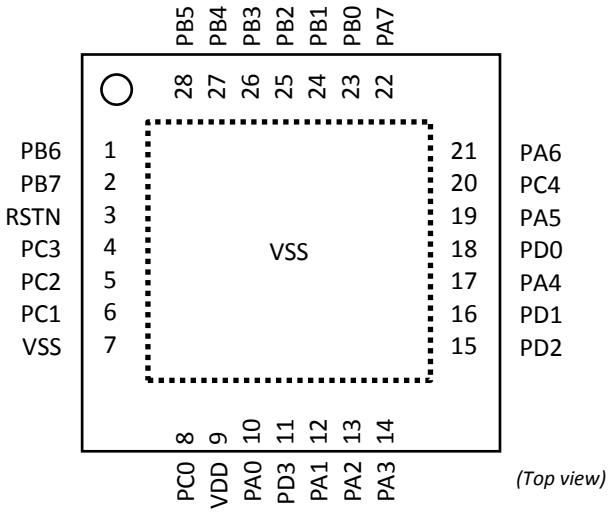
(Top view)

(QFN24)



(Top view)

(QFN28)



(Top view)

Pin	Function	Timer / PWM	Communication	Other	Analogue (Ch.0/Ch.1)
PA0	Full feature GPIO w/ Interrupt	T0/T24EX/T24CC	-	-	ADC V+ / ADC V-
PA1	Full feature GPIO w/ Interrupt	T2EX	SDA (I^2C)	-	ADC V+ / ADC V-
PA2	Full feature GPIO w/ Interrupt	T2/T2OUT	SCK (I^2C)	CNVSTR (ADC)	ADC V+ / ADC V-
PA3	Full feature GPIO w/ Interrupt	T2CC3	-	-	ADC V+ / ADC V-
PA4	Full feature GPIO w/ Interrupt	T2CC4	-	MCLK	ADC V+ / ADC V-
PA5	Full feature GPIO w/ Interrupt	T24OUT	SDO(SPI) / TX(UART0)*	-	ADC V+ / ADC V-
PA6	Full feature GPIO w/ Interrupt	T2CC1	SDI(SPI) / RX(UART0)*	-	ADC V+ / ADC V-
PA7	Full feature GPIO w/ Interrupt	T2CC2	SCK(SPI)	-	ADC V+ / ADC V-
PB0	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PB1	Full feature GPIO w/ Interrupt	T1	-	SL (ISP-SL)	ADC V+ / ADC V-
PB2	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC VREF-
PB3	Full feature GPIO w/ Interrupt	T24CB	-	-	ADC V+ / ADC V-
PB4	Full feature GPIO w/ Interrupt	T24CA/PWM0	-	-	ADC V+ / ADC V-
PB5	Full feature GPIO w/ Interrupt	-	TX (UART0)	-	ADC V+ / ADC V-
PB6	Full feature GPIO w/ Interrupt	-	RX (UART0)	-	ADC V+ / ADC V-
PB7	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PC0	Full feature GPIO w/ Interrupt	PWM1	-	-	ADC VREF+ / ADC V-
PC1	Full feature GPIO w/ Interrupt	REM (CA)	-	-	ADC V+ / ADC V-
PC2	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PC3	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PC4	Full feature GPIO w/ Interrupt	-	-	-	ADC V+ / ADC V-
PD0	Full feature GPIO w/ Interrupt	-	TX (UART1)	-	-
PD1	Full feature GPIO w/ Interrupt	-	RX (UART1)	-	-
PD2	Full feature GPIO w/ Interrupt	-	-	-	-
PD3	Full feature GPIO w/ Interrupt	-	-	-	-

*: Available by enabling software setting in DC6288FT (8/16/32) N3L only

Pin	Function	Remarks	Other
RSTN	External Reset (Active-low)	Capacity load must be <50pF	ECLK (ISP-SL)
VDD	MCU Power Supply	Require 100uF + 0.1uF decoupling capacitor	-
VSS	MCU Power Ground		-

3 Architecture Overview

DC6288FT is an 8-bit Microcontroller Unit (MCU) with low voltage embedded Flash memory, internal high accuracy RC oscillator, digital peripherals, analogue to digital converter (ADC) and more for general low power or handheld application.

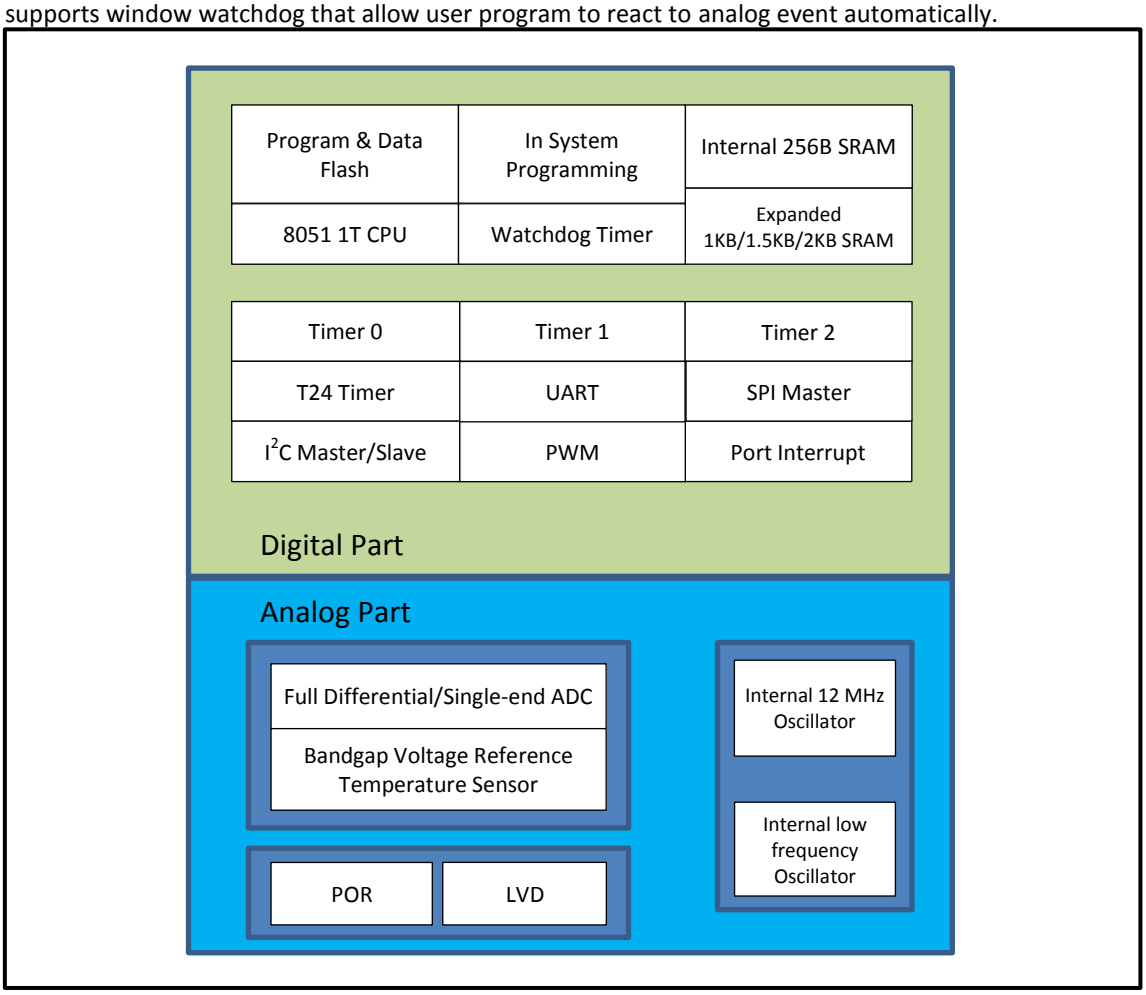
As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

The internal RC oscillator can generate clock signal without any external components, and provide an accurate system clock that is trimmed from factory or by In-system Programmer during MCU programming for a more precise clocking.

The MCU also comes with array of timers/counters that can be configured for varies timing or counting needs. There are also capable for generate pulse width modulation signals automatically, allowing system control via analogue means.

The built-in communication peripherals provide an automated support for standard protocols used for module to module communication.

The 12 bit full differential, or 11 bit single-ended, successive approximation ADC with IO channel multiplexing provides a fast, accurate, and flexible analogue to digital interface for connecting the sensors to the MCU. It supports single, continuous, timer, or external event conversion mode. It also supports window watchdog that allow user program to react to analog event automatically.



4 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

5 Memory

Memory comprises of the following elements, namely:

- 8KB/16KB/32KB Flash memory for Code and Data usage
- 256B Internal SRAM
- 1KB/1.5KB/2KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

The embedded Flash memory can be partitioned for program or data memory use in 512 byte interval. It can be read and write by user program via the built-in Flash controller peripheral. In addition, the write operation is protected by write protection signature to avoid writing accidentally.

6 I/O port

There are 4 GPIO ports on the MCU, Port A/B/C/D, and each port have varies number of pins depends on package.

The 20-pin TSSOP package has one 8-bit port (PORTA), one 6-bit port (PORTB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

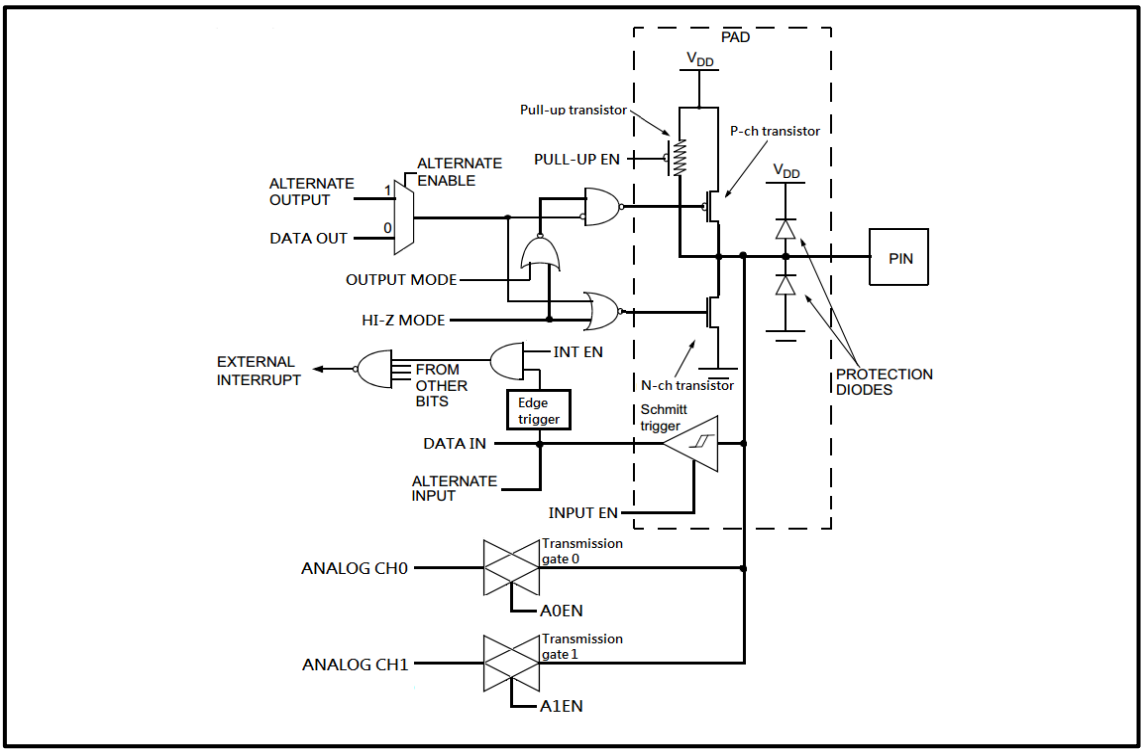
The 20-pin QFN package has two 8-bit ports (PA and PB) and one 1-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

The 24-pin package has two 8-bit ports (PA and PB) and one 5-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

The 28-pin package has two 8-bit ports (PA and PB), one 5-bit port (PORTC), and one 4-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines.

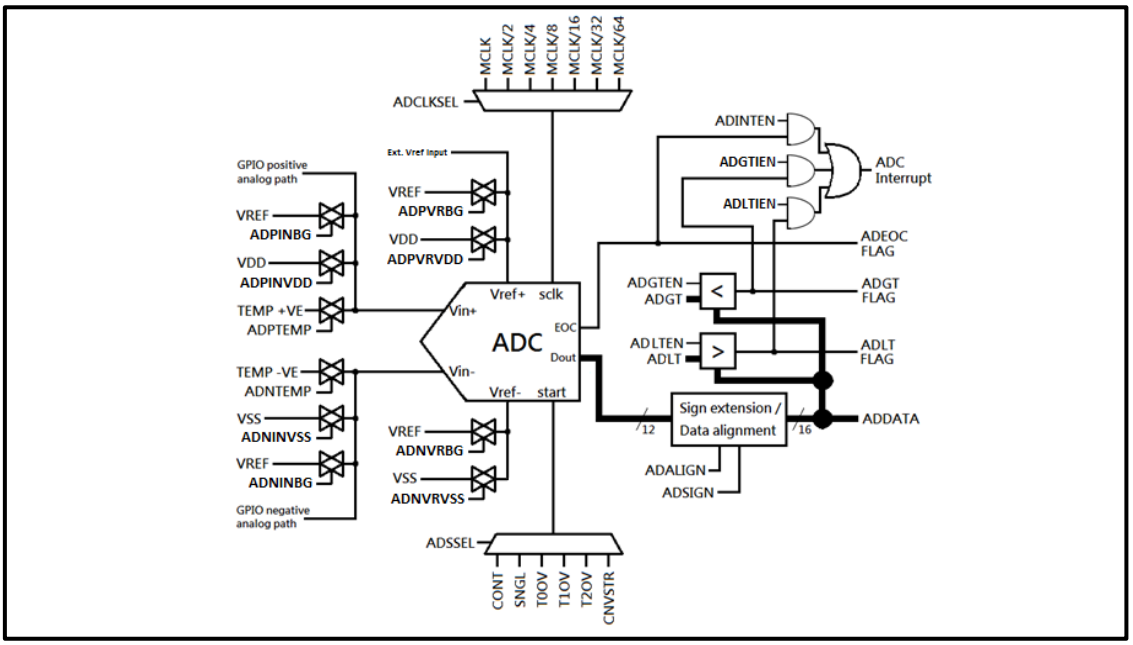
Each individual pin has the following feature that can be configure independently:

- Digital output mode (High impedance, push-pull, and open-drain mode)
- Pull-up resistor
- Input Schmitt trigger
- Interrupt trigger (Rising, falling, or both edge)
- Analogue channels



7 12-Bit Full-differential/11-bit Single-end ADC

The 12-bit Full-differential/11-bit Single-end ADC module consists of two input paths, V+ and V-, to digitize full differential signal at maximum conversion rate of 200ksps. It can also be configured to measure signal-end input with 11-bit resolution. The start of conversion can be triggered by register, timer overflow or external rising-edge. The reference voltage (VREF) is also selectable from either internal, external or VDD by software configurations.



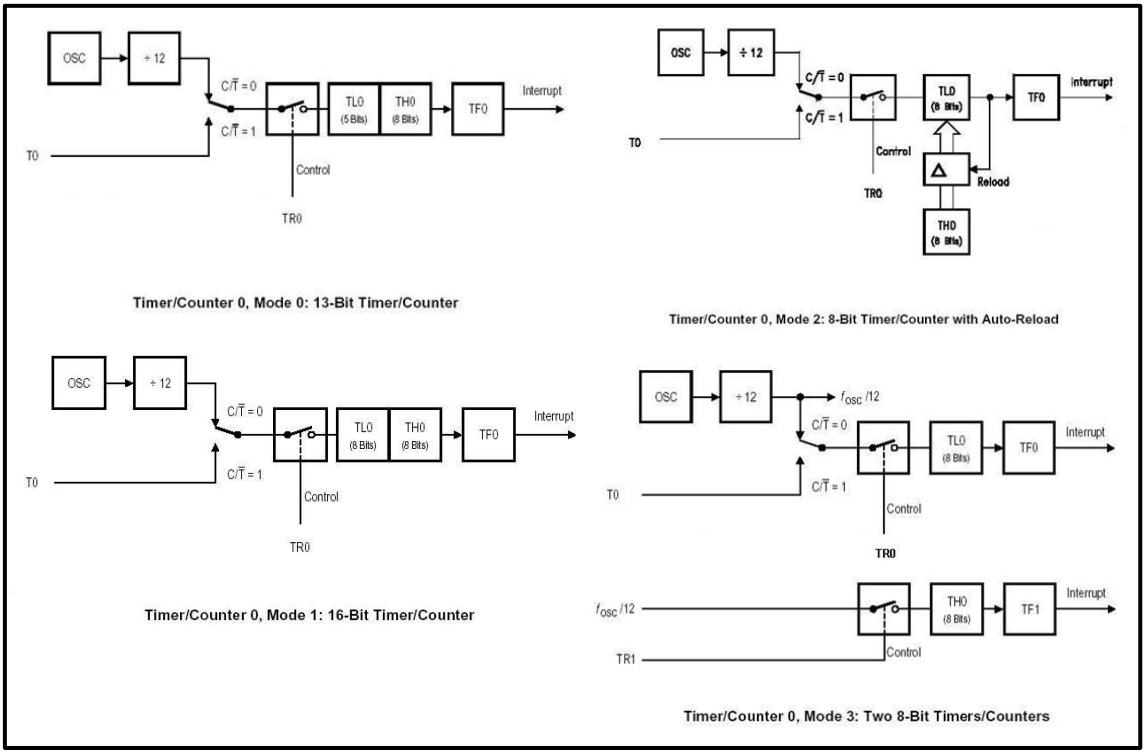
8 Internal Bandgap Voltage Reference & Temperature Sensor

The internal bandgap voltage reference can provide a fix voltage which can be used for voltage comparison and measurement. The internal temperature sensor uses the ADC to sense the on-chip temperature without external component.

9 General Purpose Timers/Counters 0 & 1

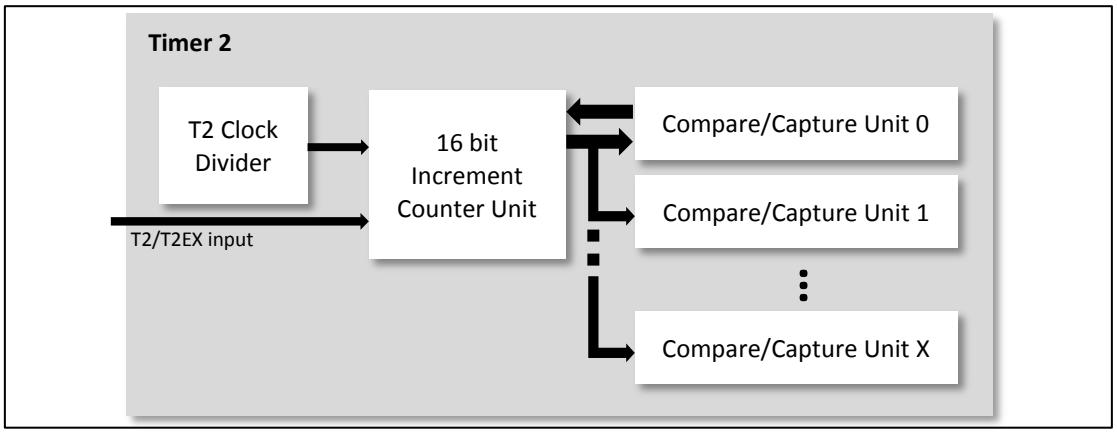
Three independent general purpose 16-bit timers/counters, Timer0, and Timer1 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.



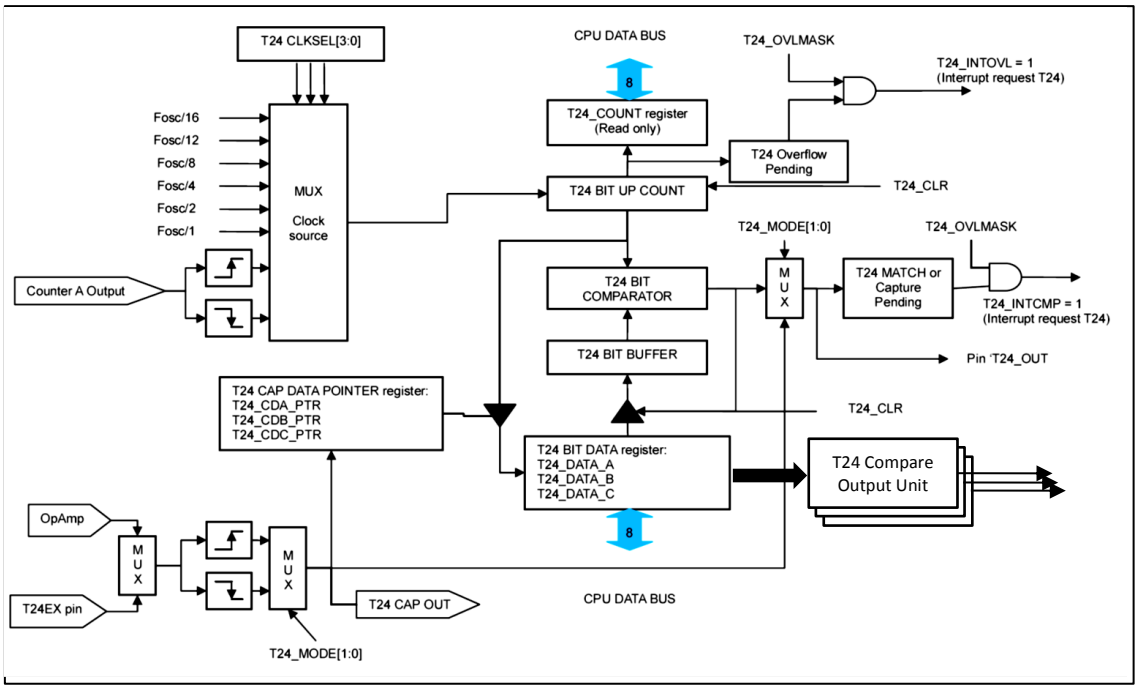
10 **Timer 2**

Timer 2 consists of a 16-bit timer/counter unit and multiples of compare/capture units. The timer unit itself is capable as a 16-bit system timer/counter, or an external event timer/counter. It also provides the base counter value to the compare/capture units, where each compare/capture unit can act as a system clock timer, external event timer, or PWM output generator.



11 **Timer 24**

Timer 24 is a 24 bit timer that provides high resolution and counting length designed to capture Infra-red signal carrier frequency as high as 500kHz for event 2 seconds apart. In capture mode, there is 3 capture registers that can time 3 events automatically without servicing. It can also operate as interval timer mode and compare mode which can generates interrupt for timing purposes, and/or pulse width modulation (PWM) outputs.



12 Enhanced UART

The UART controller is fully compatible with the standard 8051 serial channel with enhancement. The UART perform framing error detection and automatic address recognition in all four modes (one synchronous and three asynchronous. It supports multiprocessor communication as does the standard 80C51 UART.

13 Inter-Integrated Circuit (I^2C) Interface

The I^2C Bus Controller supports all transfer modes from and to the I^2C bus and transfers up to 100kbit/s in the standard mode or up to 400kbit/s in the fast mode. The I^2C logic handles bytes transfer autonomously which keeps track of serial transfers, with status registers reflect the status of the I^2C Bus Controller and the I^2C bus to applications. The interface also supports the System Management Bus (SMBus) protocol where additional timeout detection is added.

14 Serial Peripheral Interface

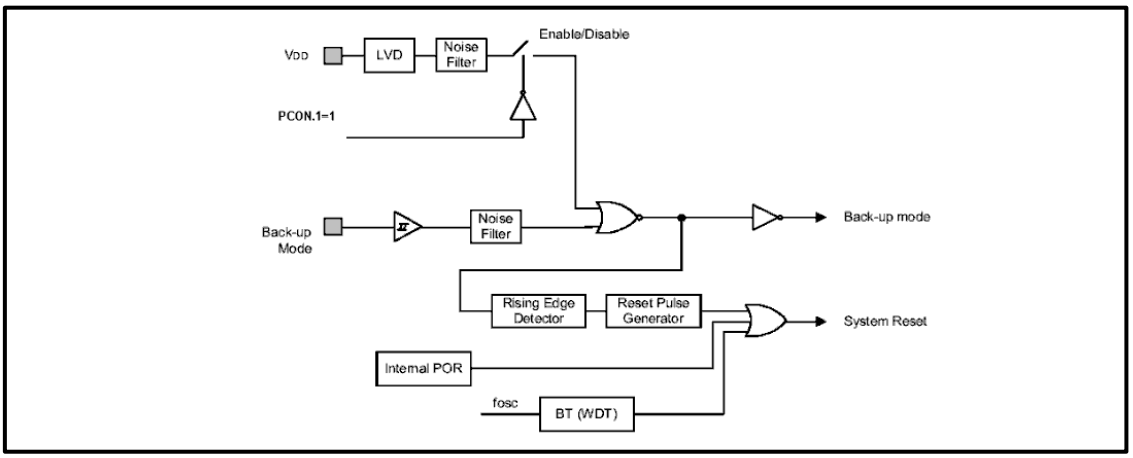
The integrated master mode Serial Peripheral Interface (SPI) controller allows data to be synchronously transmitted and received simultaneously with bit rate up to 4Mbits/s between multiple external peripherals.

15 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



16 In System Programming

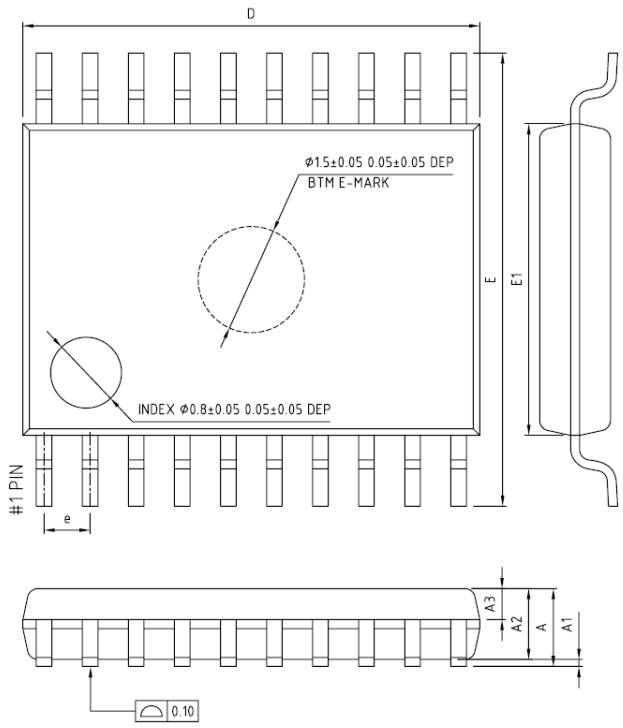
The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. The DC6288FT series support ISP-SL protocol which requires only a 2 wire bus to perform the ISP function, minimize the impact on application design.

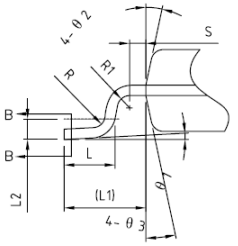
17 Ordering Information

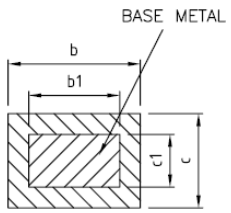
Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6288FT8N3L	TSSOP20	8KB Configurable (Program + Data)		256B + 1KB	13
DC6288FT8N3M	TSSOP20	8KB Configurable (Program + Data)		256B + 1KB	17
DC6288FT8N3R	TSSOP20	8KB Configurable (Program + Data)		256B + 1KB	17
DC6288FT8Y3L	TSSOP24	8KB Configurable (Program + Data)		256B + 1KB	17
DC6288FT8N6	QFN20	8KB Configurable (Program + Data)		256B + 1KB	17
DC6288FT8Y6	QFN24	8KB Configurable (Program + Data)		256B + 1KB	21
DC6288FT8U6	QFN28	8KB Configurable (Program + Data)		256B + 1KB	25
DC6288FT16N3L	TSSOP20	16KB Configurable (Program + Data)		256B + 1.5KB	13
DC6288FT16N3M	TSSOP20	16KB Configurable (Program + Data)		256B + 1.5KB	17
DC6288FT16N3R	TSSOP20	16KB Configurable (Program + Data)		256B + 1.5KB	17
DC6288FT16Y3L	TSSOP24	16KB Configurable (Program + Data)		256B + 1.5KB	17
DC6288FT16N6	QFN20	16KB Configurable (Program + Data)		256B + 1.5KB	17
DC6288FT16Y6	QFN24	16KB Configurable (Program + Data)		256B + 1.5KB	21
DC6288FT16U6	QFN28	16KB Configurable (Program + Data)		256B + 1.5KB	25
DC6288FT32N3L	TSSOP20	32KB Configurable (Program + Data)		256B + 2KB	13
DC6288FT32N3M	TSSOP20	32KB Configurable (Program + Data)		256B + 2KB	17
DC6288FT32N3R	TSSOP20	32KB Configurable (Program + Data)		256B + 2KB	17
DC6288FT32Y3L	TSSOP24	32KB Configurable (Program + Data)		256B + 2KB	17
DC6288FT32N6	QFN20	32KB Configurable (Program + Data)		256B + 2KB	17
DC6288FT32Y6	QFN24	32KB Configurable (Program + Data)		256B + 2KB	21
DC6288FT32U6	QFN28	32KB Configurable (Program + Data)		256B + 2KB	25

18 Package Outlines

18.1 20-pin TSSOP







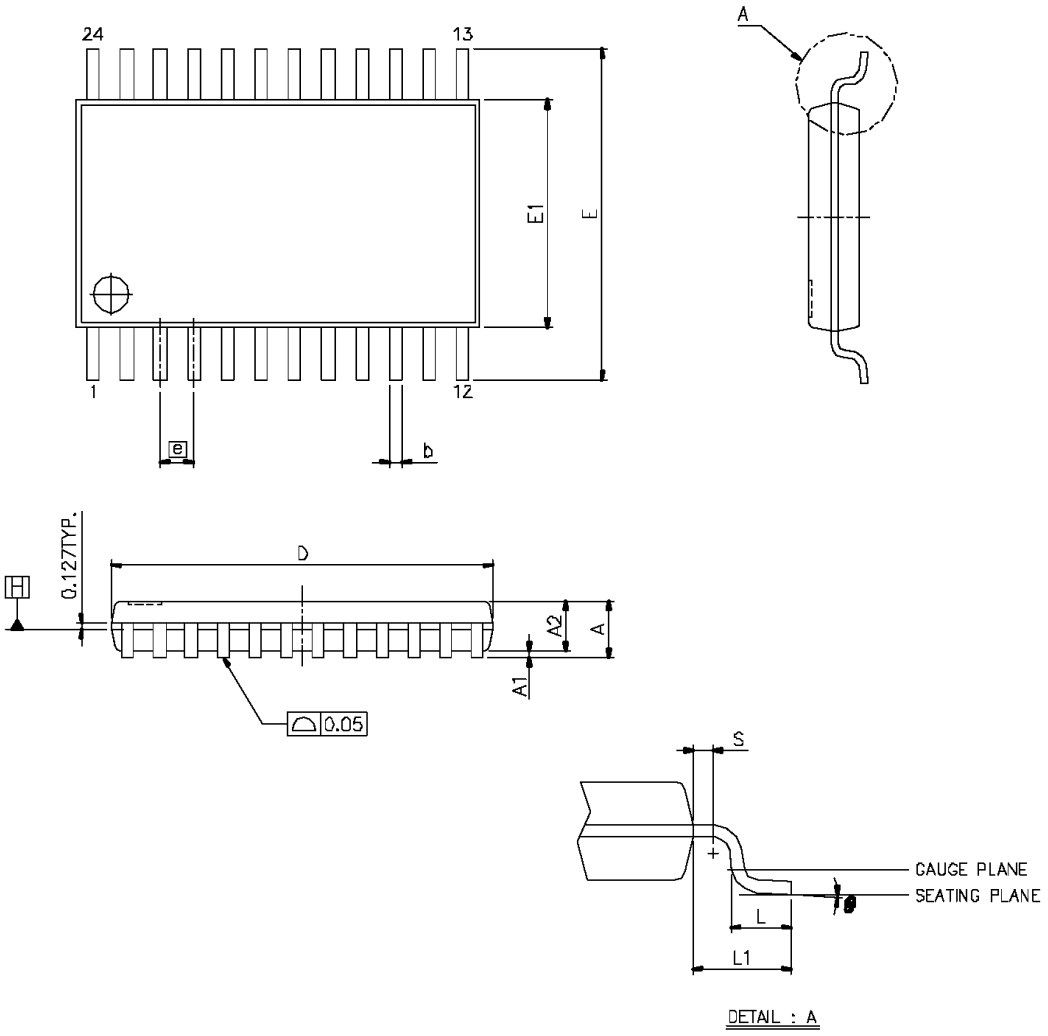
SECTION B–B

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ 1	0°	–	8°
θ 2	10°	12°	14°
θ 3	10°	12°	14°

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

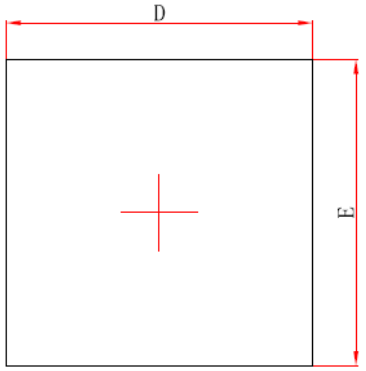
18.2 24-pin TSSOP



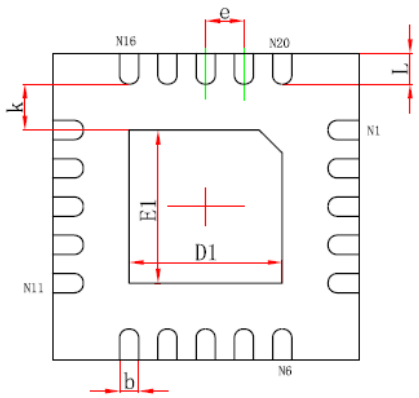
SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
D	7.70	7.80	7.90
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°

Dimensions in millimeters

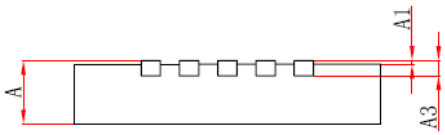
18.3 20-pin QFN



Top View



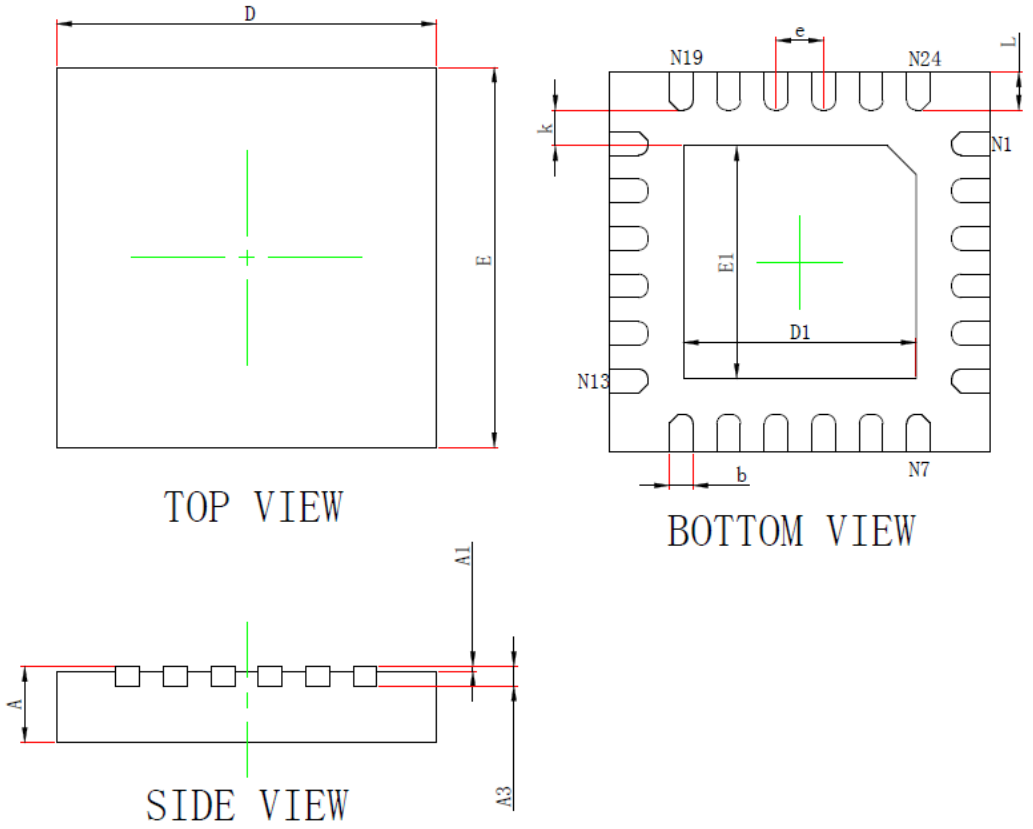
Bottom View



Side View

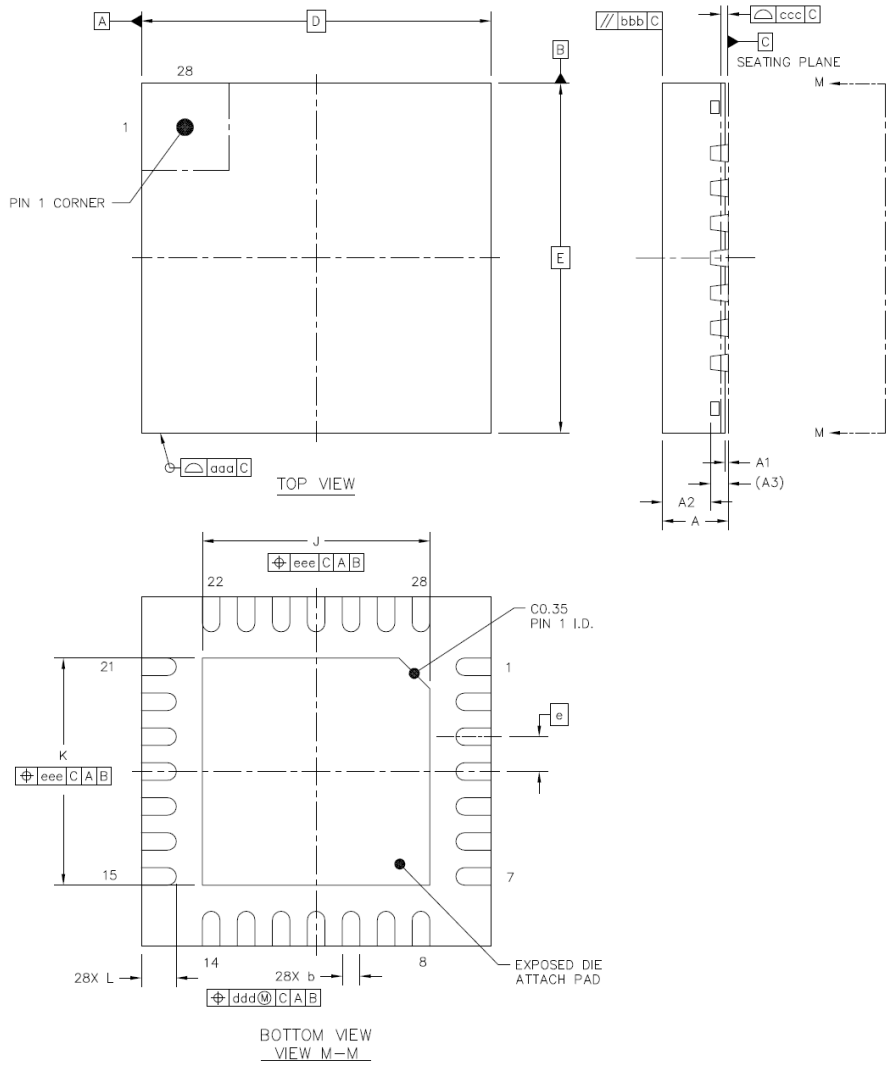
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.924	4.076	0.154	0.160
E	3.924	4.076	0.154	0.160
D1	1.900	2.100	0.075	0.083
E1	1.900	2.100	0.075	0.083
k	0.200MIN.		0.008MIN.	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.324	0.476	0.013	0.019

18.4 24-pin QFN



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A3	0.203REF.		0.008REF.	
D	3.950	4.050	0.156	0.159
E	3.950	4.050	0.156	0.159
E1	2.400	2.500	0.094	0.098
D1	2.400	2.500	0.094	0.098
k	0.200MIN		0.008MIN	
b	0.200	0.300	0.008	0.012
e	0.500TYP.		0.020TYP.	
L	0.350	0.450	0.014	0.018

18.5 28-pin QFN



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.7	0.75	0.8
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	J	2.5	2.6	2.7
	Y	K	2.5	2.6	2.7
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

19 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
0.6	May, 2016	-	-	Update to latest design	Patrick Li	
0.72	Aug, 2017			Combined DC6288FT8/16/32	Patrick Chan	
0.9	Feb 2018			Added QFN20 and QFN24 pin assignment Changed 16MHz to 12MHz	Patrick Chan	
1.0	Mar 2018			Changed 6688FTxY6 to 6288FTxY6	Patrick Chan	
1.1	Mar 2018			Updated QFN24 pin assignment	Patrick Chan	
1.2	Jun 2018			Updated ADC specification	Patrick Li	
1.3	Dec 2018			Added QFN28 pin assignment	Patrick Chan	
1.4	May 2019			Added TSSOP20(L) pin assignment	Patrick Chan	Danny Ho
1.5	May 2019			Added thermal resistance	Patrick Chan	
1.6	Aug 2019			Revised package thermal resistance values Added TSSOP24 pin assignment	Patrick Chan	

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Dragonchip Ltd.
TEL: (852) 2776-0111
FAX: (852) 2776-0996
http://www.dragonchip.com

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