DC6388FD

LCD Microcontroller

DC6388FD is an 8-bit Microcontroller Unit designed for handheld product application with LCD display. It is manufactured in advanced CMOS process with 1T 8051 CPU core, embedded flash memory, on-chip LCD driver and peripherals suitable for LCD IR remote controller. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Memory
  - 32KB Configurable Program & Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 512B SRAM
- Built-in LCD Controller / Driver
  - 48-Pin Package: 29 Segment x 4 Common
  - 52-Pin Package: 32 Segment x 4 Common
  - 64-Pin Package: 40 Segment x 4 Common / 36 Segment x 8 Common
- IR generator by counter A with auto-reload function
- 4 priority level interrupt controller
- 36 bit-programmable I/O ports
- I/O port with interrupt function
- 16-bit Timers x 3
- 20-bit RTC Timer
- 16-bit Watchdog Timer
- Standard UART
- I2C Master
- Clock Generating Circuits
  - XIN clock: 4MHz typical (ceramic / crystal resonator)
  - XIN2 clock: 32.768kHz typical (crystal resonator)
  - Internal low-frequency oscillator: 50kHz typical
- Low Voltage Detection (LVD) for back-up mode
- Low Voltage Indicator (LVI)
- Operating temperature: -40°C to +85°C
- Max operating voltage: 3.6V
- Package type:
  - 48-pin LQFP (7x7mm)
  - 52-pin LQFP (10x10mm)
  - 64-pin LQFP (7x7mm)

Quick look on Ordering Information

Table of Contents

1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B C, D and E[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B C, D and E[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of the I/O pin when configured to push-pull output high.
[2] It is measured as total for Ports A, B, C, D and E when configured to push-pull output high.
[3] It is measured for any one of the I/O pin when configured to push-pull output low.
[4] It is measured as total for Ports A, B, C, D and E when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input pins except XIN and XIN2	0.7 V_{DD}	-	V_{DD}	V
	V_{IH2}	XIN, XIN2	V_{DD} – 0.3	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins except XIN and XIN2	0	-	0.3 V_{DD}	V
	V_{IL2}	XIN, XIN2	0	-	0.3	V
Output High Voltage	V_{OH1}	All output pins except Port C1, V_{DD} = 3.0V, I_{OH} = - 10mA, T_A = 25°C	V_{DD} – 0.9	-	-	V
	V_{OH2}	Port C1, V_{DD} = 3.0V, I_{OH} = - 12mA, T_A = 25°C	V_{DD} – 0.9	-	-	V
Output Low Voltage	V_{OL1}	All output pins except Port C1, V_{DD} = 3.0V, I_{OL} = 10mA, T_A = 25°C	-	-	0.9	V
	V_{OL2}	Port C1, V_{DD} = 3.0V, I_{OL} = 14mA, T_A = 25°C	-	-	0.9	V
Input High Leakage Current	I_{LIH1}	All input pins except XIN, XOUT, XIN2, XOUT2 and ISPSEL, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	XIN, XOUT, XIN2 and XOUT2; V_{IN} = V_{DD}	-	-	20	µA
	I_{LIH3}	ISPSEL, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins except XIN, XOUT, XIN2 and XOUT2; V_{IN} = 0	-	-	-1	µA
	I_{LIL2}	XIN, XOUT, XIN2 and XOUT2; V_{IN} = 0	-	-	-20	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Pull-up Resistors	R_{PU}	V_{DD} = 3.0V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Supply Current Run Mode[1][2]	I_{DDRM}	MCLK = XIN clock[2] f_{XIN} = 4MHz[2][3] V_{DD} = 3.0V, T_A = 25°C	-	5.5	6.5	mA
		MCLK = XIN2 clock[2] f_{XIN2} = 32.768kHz[2][4] V_{DD} = 3.0V, T_A = 25°C	-	28	45	uA
		MCLK = int. low-freq. osc. clock[2] f_{LF} = 50kHz[2][5] V_{DD} = 3.0V, T_A = 25°C	-	30	45	uA
Supply Current Idle Mode[1][2]	I_{DDIM}	MCLK = XIN clock[2] f_{XIN} = 4MHz[2][3] V_{DD} = 3.0V, T_A = 25°C	-	3.5	4.5	mA
		MCLK = XIN2 clock[2] f_{XIN2} = 32.768kHz[2][4] V_{DD} = 3.0V, T_A = 25°C	-	22	35	uA
		MCLK = int. low-freq. osc. clock[2] f_{LF} = 50kHz[2][5] V_{DD} = 3.0V, T_A = 25°C	-	22	35	uA
Supply Current Stop Mode[1][2]	I_{DDSM}	LCLK = XIN2 clock[2] f_{XIN2} = 32.768kHz[2][4] V_{DD} = 3.0V, T_A = 25°C	-	10	15	uA
		LCLK = int. low-freq. osc. clock[2] f_{LF} = 50kHz[2][5] V_{DD} = 3.0V, T_A = 25°C	-	4	10	uA
		f_{XIN} = stop f_{XIN2} = stop f_{LF} = stop[2] V_{DD} = 3.0V, T_A = 25°C	-	2	5	uA

Remarks:

[1] Total current consumed through V_{DD}. It includes the input leakage current when the level of the input pin is fixed to V_{DD} or V_{SS} but it does not include the current consumed by LVD circuit, internal pull-up resistors and LCD driver.

[2] MCLK: Main system clock
LCLK: Subsystem clock
f_{XIN}: XIN clock frequency
f_{XIN2}: XIN2 clock frequency
f_{LF}: Internal low-frequency oscillator clock frequency

[3] When XIN2 clock and internal low-frequency oscillator clock are stopped (f_{XIN2} = stop, f_{LF} = stop).

[4] When XIN clock and internal low-frequency oscillator clock are stopped (f_{XIN} = stop, f_{LF} = stop).

[5] When XIN clock and XIN2 clock are stopped (f_{XIN} = stop, f_{XIN2} = stop).

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Program setting[2]	1.65	1.80	1.95	V
		Default setting[2]	2.00	2.15	2.30	V
		Program setting[2]	2.35	2.50	2.65	V
		Program setting[2]	2.65	2.80	2.95	V
Low Voltage Detect Level	V_{LVD1}		1.5	1.6	1.7	V

Remarks:

[1] $\Delta V = V_{LVD2} - V_{LVD1}$

[2] Configurable by register LVIL[1:0]. For more details, refer to the register definition of the user guide document.

1.4 LCD Driver

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal dividing resistor for LCD power supply	R_{LCD}	RSEL = 1, V_{DD} = 3.0V	-	100	-	kΩ
		RSEL = 0, V_{DD} = 3.0V	-	200	-	kΩ
COM output impedance	R_{COM}	V_{DD} = 3.0V	-	2	-	kΩ
SEG output impedance	R_{SEG}	V_{DD} = 3.0V	-	2	-	kΩ

1.5 SRAM Data Retention Voltage in Stop Mode

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Stop Mode	-	-	1	uA

1.6 Input / Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}		-	-	10	pF
I/O Capacitance	C_{IO}		-	-	10	pF

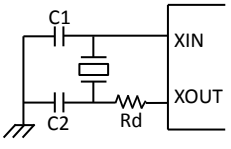
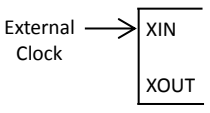
1.7 Flash Memory Data Retention

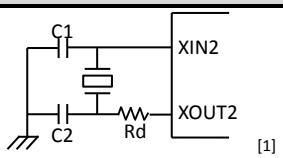
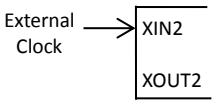
(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.8 Oscillation Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Condition	Clock Circuit	Min	Typ	Max	Unit
XIN clock frequency (crystal / ceramic resonator)	f_{XIN}	-	 [1]	1	-	16.5	MHz
XIN clock frequency (external clock input)	f_{XIN}	-		1	-	16.5	MHz

Parameter	Symbol	Condition	Clock Circuit	Min	Typ	Max	Unit
XIN2 clock frequency (crystal resonator)	f_{XIN2}	-	 [1]	-	32.768	-	kHz
XIN2 clock frequency (external clock input)	f_{XIN2}	-		-	32.768	-	kHz
Internal low-frequency oscillator clock frequency[2]	f_{LF}	T_A = -20°C to +85°C	-	25	50	75	kHz

[1] For the components selection in this circuit, please refer to the matching report from resonator manufacturer.
[2] Without trimming

(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
XIN clock stabilization time (crystal resonator)	t_{XINS}	f_{XIN} > 1MHz[1] Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range	-	-	20	ms
XIN clock stabilization time (ceramic resonator)	t_{XINS}		-	-	10	ms
XIN clock stabilization time (external clock input)	t_{XINS}	XIN input High and Low width(t_{XL}, t_{XH})	25	-	500	ns
XIN2 clock stabilization time (crystal resonator)	t_{XIN2S}	f_{XIN2} = 32.768kHz[1]	-	1	-	s
Internal low-frequency oscillator clock stabilization time	t_{LFS}	f_{LF} = 50kHz[1]	-	200	400	us
Main system clock (MCLK) oscillation stabilization wait time – power-on reset or LVD reset	t_{WTR}	MCLK = XIN clock[1] by default	-	$2^{19}/f_{XIN}$[1]	-	s
Main system clock (MCLK) oscillation stabilization wait time – external reset	t_{WTR}	MCLK = XIN clock[1] by default	-	$2^{19}/f_{XIN}$[1]	-	s
Main system clock (MCLK) oscillation stabilization wait time - MCU wake-up by interrupt.	t_{WTI}	MCLK = XIN clock or XIN2 clock or Internal low-frequency oscillator clock[1]	-	$2^7/f_{OSC}$ or $2^{13}/f_{OSC}$ [1][2]	-	s

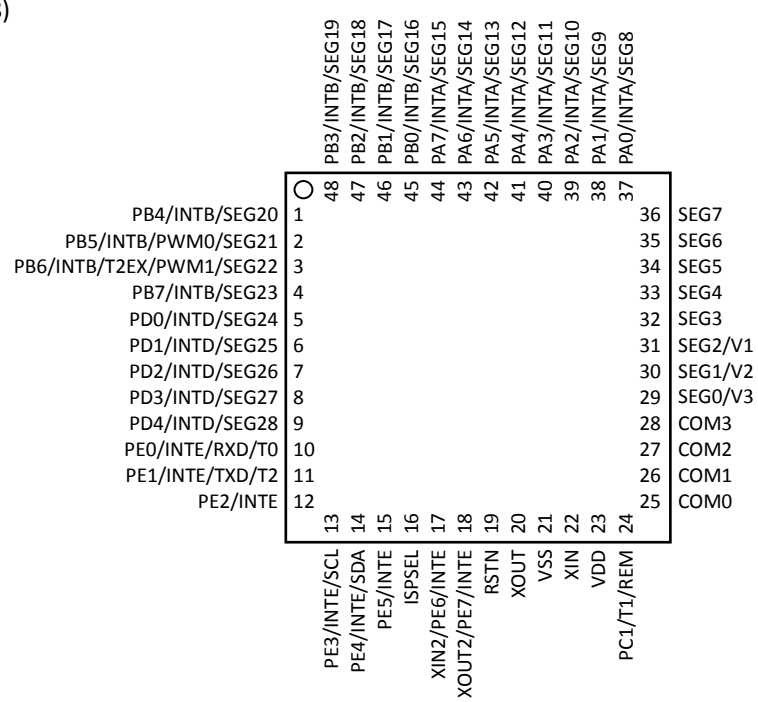
Remarks:
[1] MCLK: Main system clock
f_{OSC}: Main system clock (MCLK) frequency
f_{XIN}: XIN clock frequency
f_{XIN2}: XIN2 clock frequency
f_{LF}: Internal low-frequency oscillator clock frequency
[2] Configurable by register WTI. For more details, refer to the register definition of the user guide document.

1.9 Recommend crystal resonators for XIN2

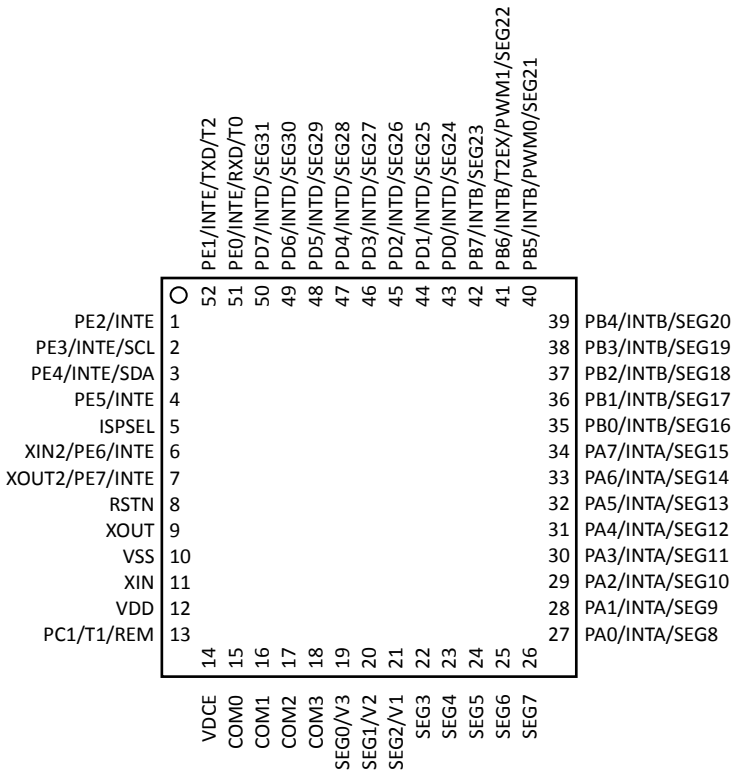
Package	Manufacturer	Part Number	Freq. (Hz)	C1/C2 (pF)	CL (pF)	ESR max (Ohm)	RT Tol. (ppm)
2T	Hong Kong X'tals Ltd	2060K3276DB01	32768	20	12.5	40000	±20
2T	Hong Kong X'tals Ltd	2060K3276DB02	32768	20	12.5	40000	±10

2 Pin Assignment

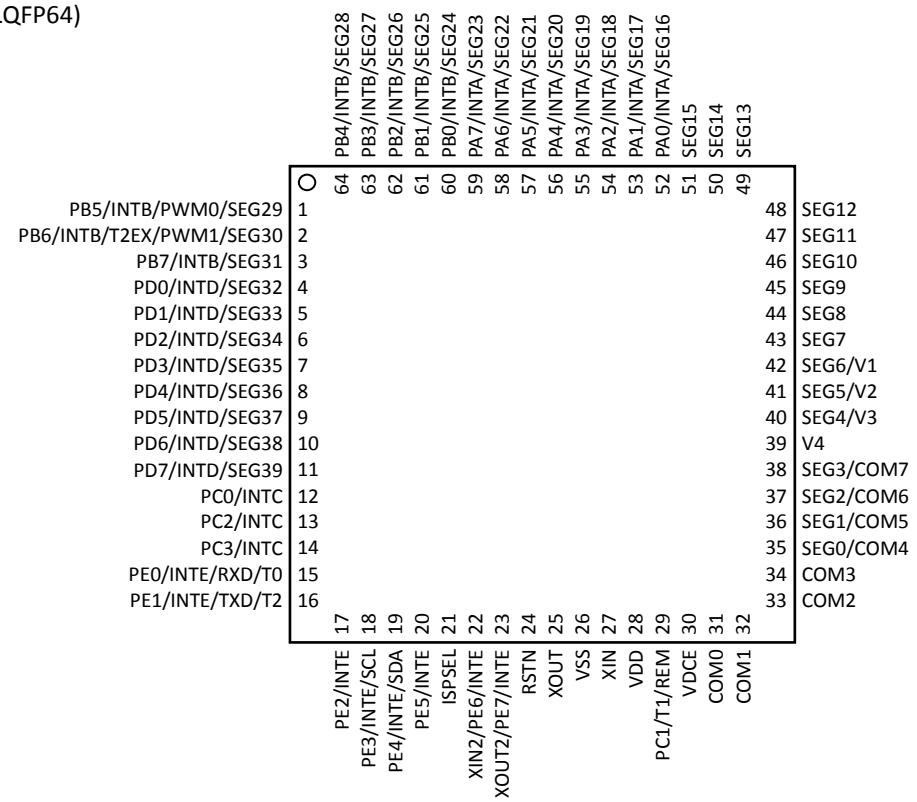
(LQFP48)



(LQFP52)



(LQFP64)



Symbol	Function
VDD	Power
VSS	Ground
RSTN	External reset
VDCE	LVD Reset enable
ISPSEL	SL (Single Line) Communication signal
XIN, XOUT	Crystal / ceramic resonator input, output
XIN2, XOUT2	Crystal resonator input, output
PA0 – PA7, PB0 – PB7, PC0 – PC3, PD0 – PD7, PE0 – PE7	Configurable input or output port
INTA, INTB, INTC, INTD, INTE	Port interrupt input
COM0 – COM7	LCD Common output
SEG0 – SEG39	LCD Segment output
REM	Counter A carrier frequency output
T0 – T2	Timer external counter input
T2EX	Timer 2 Capture-reload trigger / up down count
PWM0, PWM1	PWM output
SDA, SCL	I2C Master Serial Data, Clock
TXD, RXD	UART transmit data output, receiver data input
V1 – V4	LCD Power supply pin

3 Description

DC6388FD is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) and built-in transistor for IR remote controller application. Power management circuits such as the idle mode, stop mode and back-up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Memory

Memory comprises of the following elements, namely:

- 32KB Configurable Program & Data Flash Memory
- 256B Internal SRAM
- 512B Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

4.1 Program & Data Flash Memory

A 32KB on-chip Flash memory configurable to be used as program and data memory. It can be programmed by In-System-Programming (ISP) method.
In addition, write protection signature is available to avoid writing accidentally.

4.2 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, etc. Some locations in the SFR address space are addressable as bits.

4.3 External Function Register (XFR)

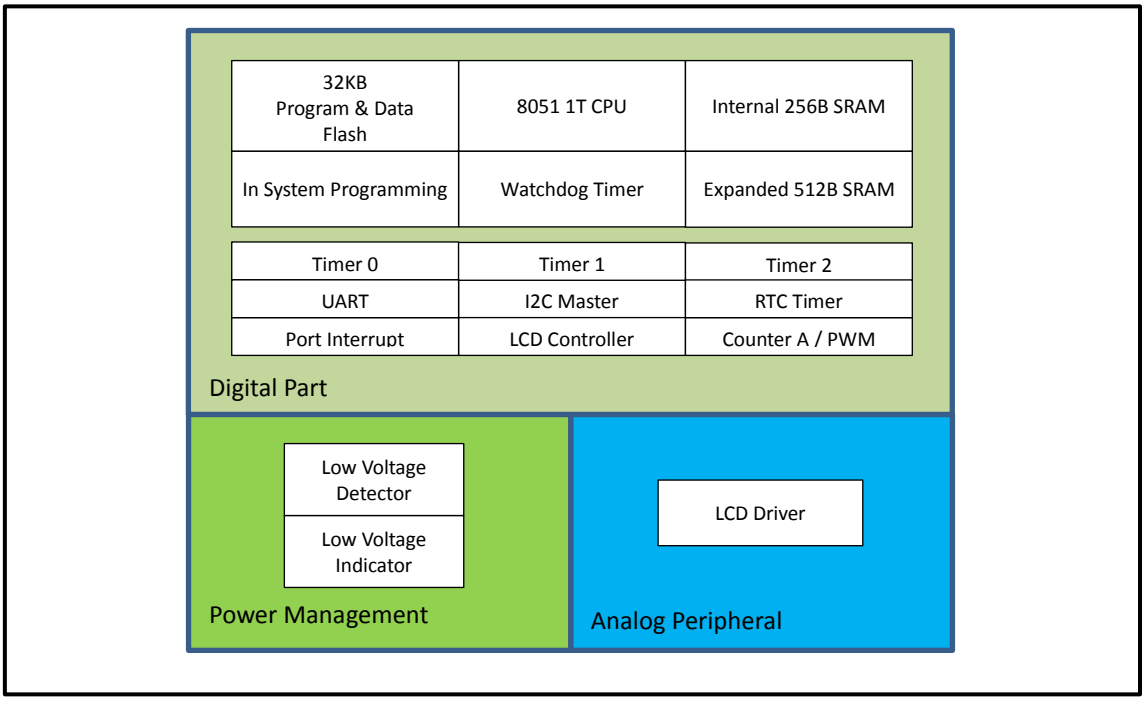
The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

5 Architecture

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8MHz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

The block diagram is illustrated in the following figure.



6 Central Processing Unit (CPU)

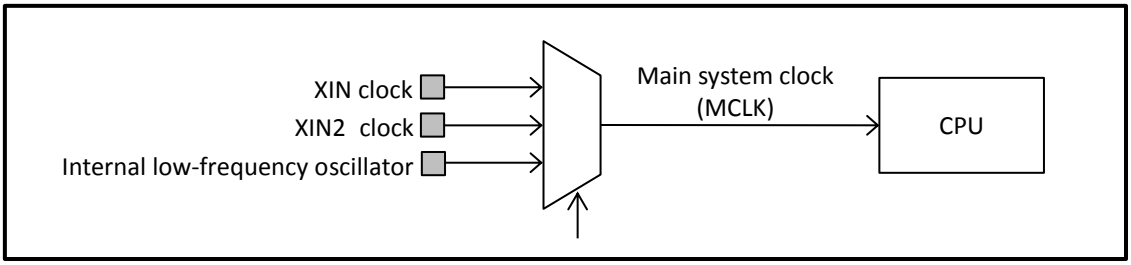
The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit

operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

Either one of the three clock sources can be supplied to CPU. For more detail clock generator diagram, refer to section 3 of the user guide.



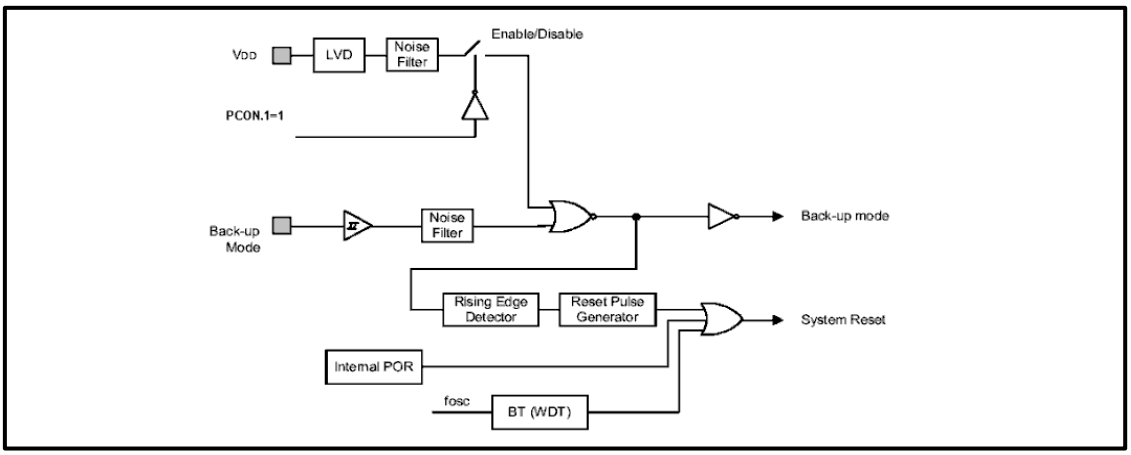
7 Low Voltage Detection Reset

The on-chip Low Voltage Detect (LVD) circuit monitors the V_{DD} voltage level and generates a system reset. It compares the voltage at pin V_{DD} with reference voltage V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC enters back-up mode at the moment "$V_{DD} = V_{LVD1}$".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "$V_{DD} >= V_{LVD2}$".

The LVD circuit provides a hysteresis ($V_{LVD2} – V_{LVD1}$) to avoid the oscillation near the decision level. To reduce the current consumption, this function can be disabled when the IC is in stop mode.

By VDCE pin, the LVD circuit is controlled by hardware externally.

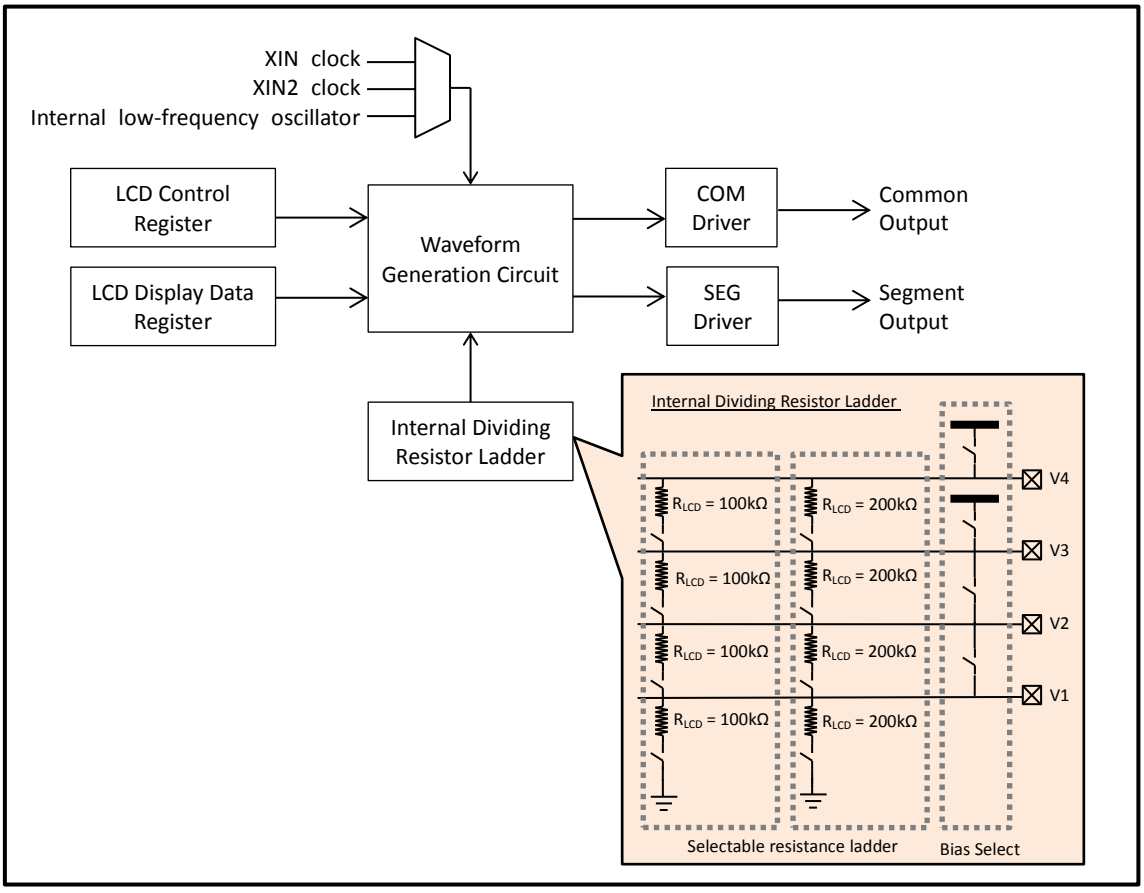


8 LCD Controller / Driver

LCD controller outputs segment and common voltages to LCD display panel, according to the on-chip display memory. Display memory is stored in the internal display RAM.

- Equip with on-chip LCD driver. Selectable resistance in 10kΩ and 100kΩ for the resistor ladder.
- Support external resistor ladder and dimming control by external variable resistor.
- 8 COM (64-pin package only)
  - ◇ 1/4 bias, 1/8 duty
  - ◇ 1/3 bias, 1/8 duty
- 4 COM Settings (48-pin, 52-pin and 64-pin package)
  - ◇ 1/2 bias, 1/2 duty
  - ◇ 1/3 bias, 1/3 duty
  - ◇ 1/3 bias, 1/4 duty
- Maximum number of displayed pixels:

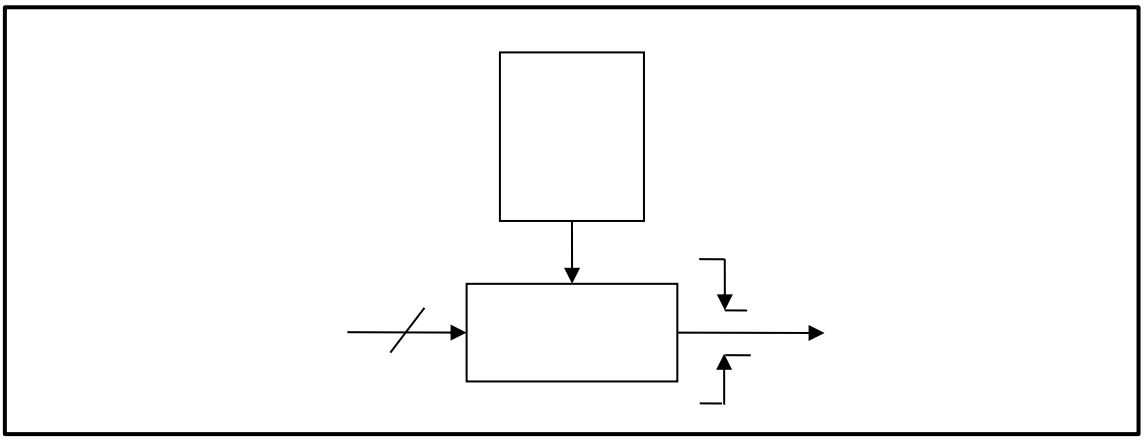
Package	Duty	Max. Display Pixels	Used COM Pins
48-pin	1/2	58 pixels	COM0 – COM1
	1/3	87 pixels	COM0 – COM2
	1/4	116 pixels	COM0 – COM3
52-pin	1/2	64 pixels	COM0 – COM1
	1/3	96 pixels	COM0 – COM2
	1/4	128 pixels	COM0 – COM3
64-pin	1/2	80 pixels	COM0 – COM1
	1/3	120 pixels	COM0 – COM2
	1/4	160 pixels	COM0 – COM3
	1/8	288 pixels	COM0 – COM7



9 I/O port

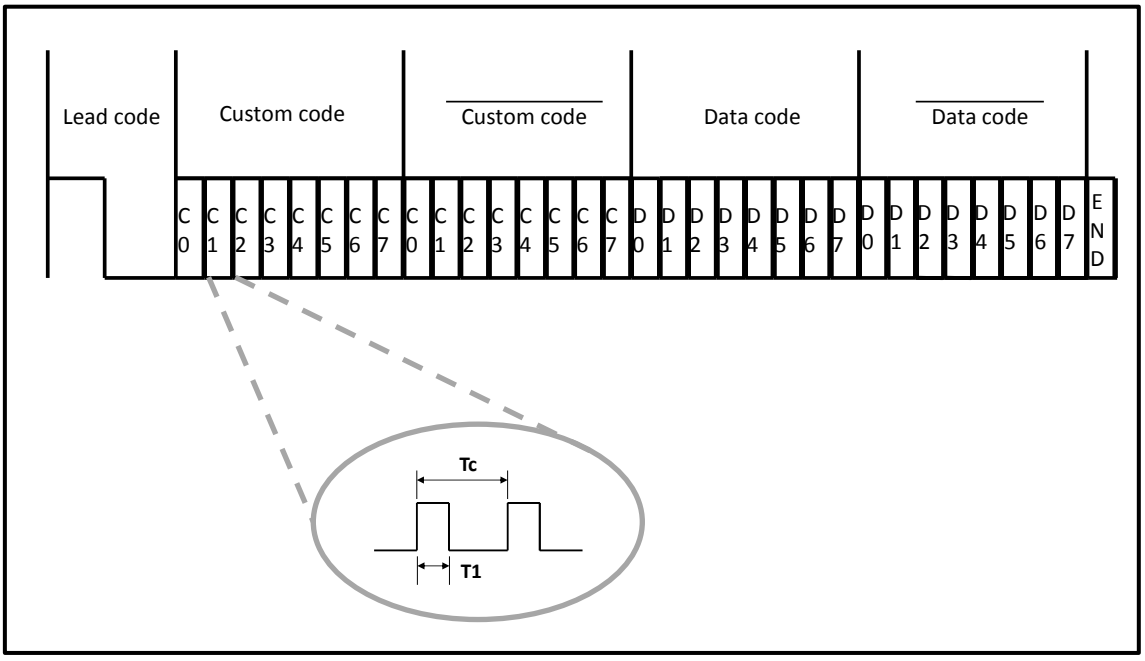
DC6388FD has four 8-bit port (port A, B, D and E) and one 4-bit port (port C). All ports are latches used to drive the bi-directional I/O lines. Upon reset, the port values are set to undetermined.

Port interrupt function is supported for port A, B, C, D and E. Pull-up resistors are included and could be assigned pin-by-pin by programming the pull-up resistor enable register.



10 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

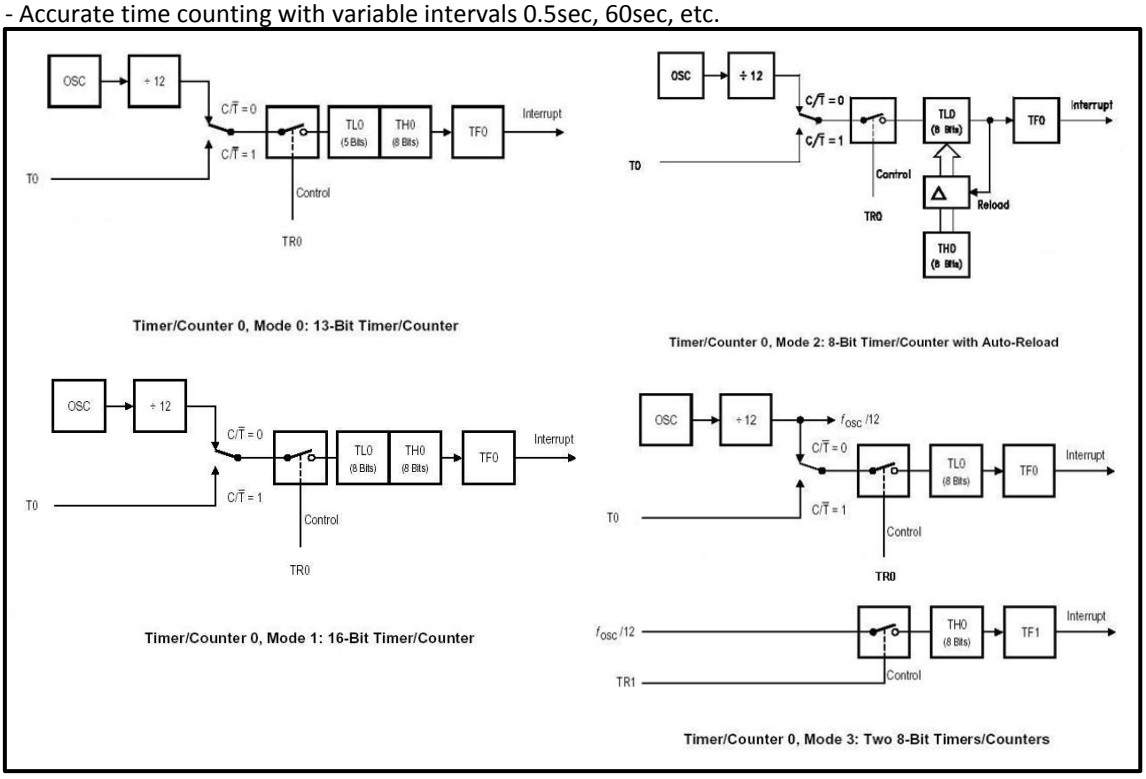
11 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator

RTC Timer is a 20-bit fixed diving frequency timer for:
- LCD driver
- LCD segment blinking
- Accurate time counting with variable intervals 0.5sec, 60sec, etc.



12 In System Programming

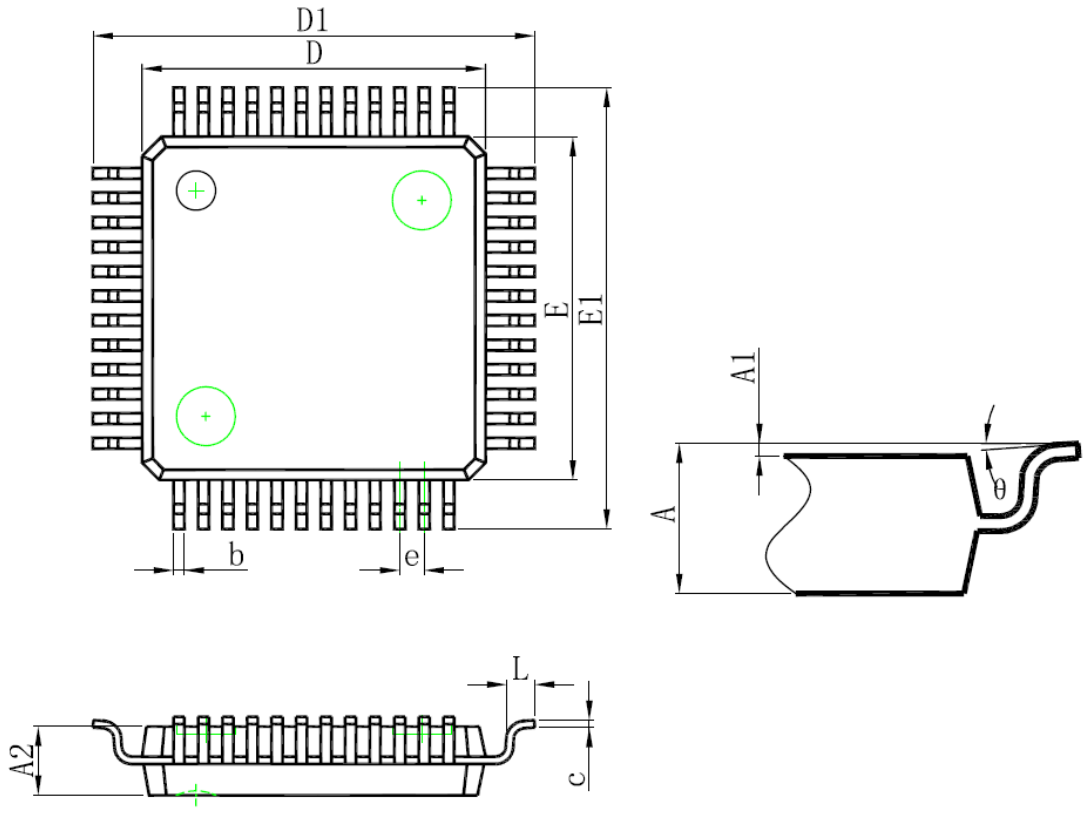
The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires only 3 wires to minimize the number of added components and board area impact.

13 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	LCD	I/O
DC6388FD32T4	LQFP48	32KB Configurable (Program + Data)		256B + 512B	29 x 4	30
DC6388FD32A4	LQFP52	32KB Configurable (Program + Data)		256B + 512B	32 x 4	33
DC6388FD32D4	LQFP64	32KB Configurable (Program + Data)		256B + 512B	40 x 4/36 x 8	36

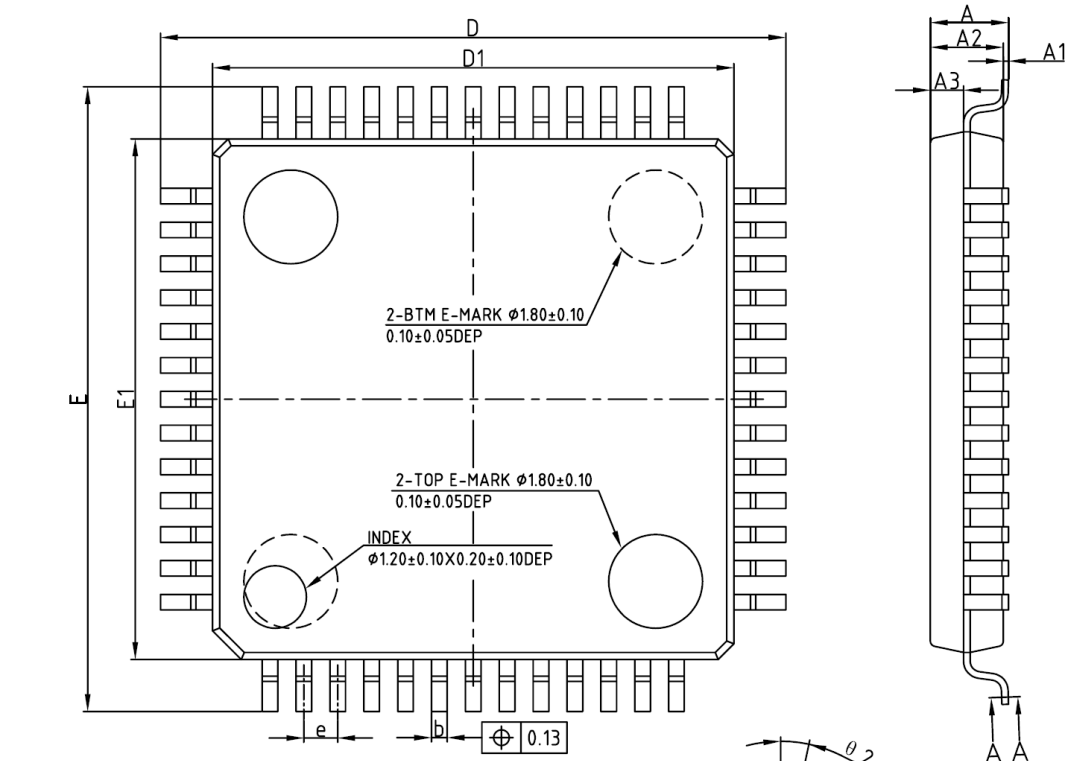
14 Package Outlines

14.1 48-pin LQFP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A		1.600		0.063
A1	0.050	0.150	0.002	0.006
A2	1.350	1.450	0.053	0.057
b	0.190	0.260	0.007	0.010
c	0.090	0.200	0.004	0.008
D	6.900	7.100	0.272	0.280
D1	8.850	9.150	0.348	0.360
E	6.900	7.100	0.272	0.280
E1	8.850	9.150	0.348	0.360
e	0.500(BSC)		0.020(BSC)	
L	0.450	0.750	0.018	0.030
θ	1°	7°	1°	7°

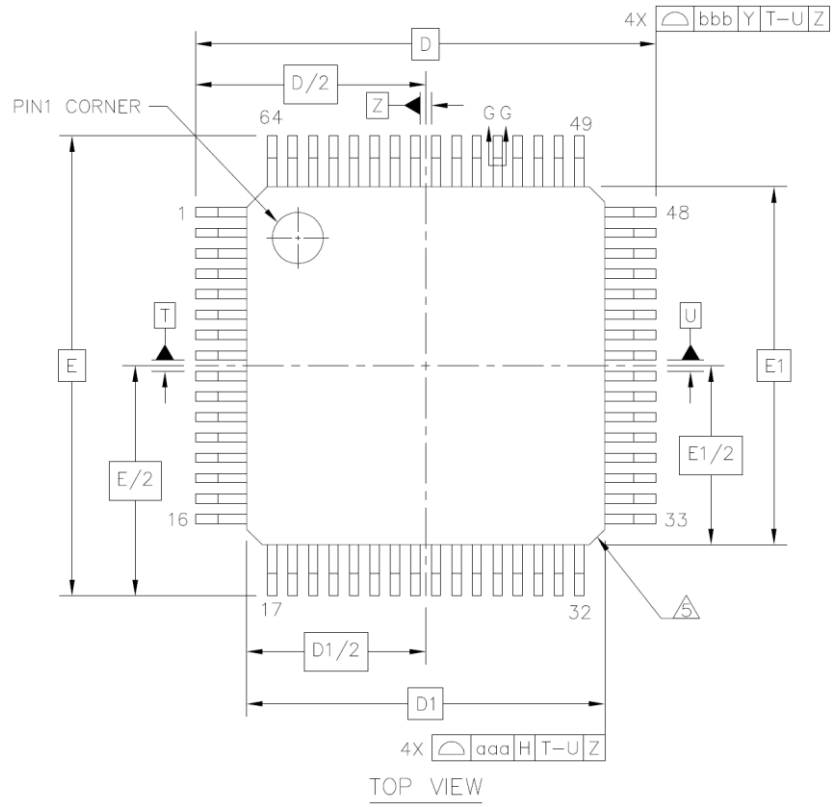
14.2 52-pin LQFP

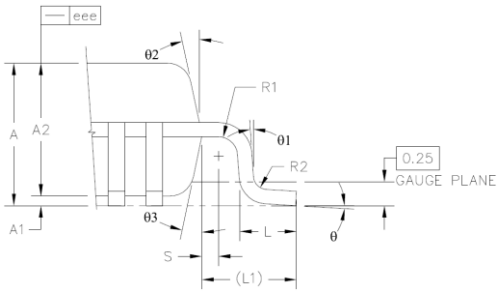


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.60
A1	0.05	–	0.20
A2	1.30	1.40	1.50
A3	0.59	0.64	0.69
b	0.28	–	0.37
b1	0.27	0.30	0.33
c	0.13	–	0.18
c1	0.12	0.13	0.14
D	11.80	12.00	12.20
D1	9.90	10.00	10.10
E	11.80	12.00	12.20
E1	9.90	10.00	10.10
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1	1.00REF		
L2	0.25BSC		
R1	0.08	–	–
R2	0.08	–	–
S	0.15	–	–
θ	0°	3.5°	7°
θ 1	0°	–	–
θ 2	11°	12°	13°
θ 3	11°	12°	13°

14.3 64-pin LQFP





		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	---	---	1.6
STAND OFF		A1	0.05	---	0.15
MOLD THICKNESS		A2	1.35	1.4	1.45
LEAD WIDTH(PLATING)		b	0.13	0.18	0.23
LEAD WIDTH		b1	0.13	0.16	0.19
L/F THICKNESS(PLATING)		c	0.09	---	0.2
L/F THICKNESS		c1	0.09	---	0.16
BODY SIZE	X	D	9 BSC		
	Y	E	9 BSC		
	X	D1	7 BSC		
	Y	E1	7 BSC		
LEAD PITCH		e	0.4 BSC		
		L	0.45	0.6	0.75
FOOTPRINT		L1	1 REF		
		θ	0°	3.5°	7°
		θ1	0°	---	---
		θ2	11°	12°	13°
		θ3	11°	12°	13°
		R1	0.08	---	---
		R2	0.08	---	0.2
		S	0.2	---	---
PACKAGE EDGE TOLERANCE		aaa	0.2		
LEAD EDGE TOLERANCE		bbb	0.2		
COPLANARITY		ccc	0.08		
LEAD OFFSET		ddd	0.07		
MOLD FLATNESS		eee	0.05		

15 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
0.1	31st Jul, 2013	All	-	First draft	Anthony Chong	Celia Ki
0.2	22nd Nov, 2013	All	-	Pin assignment and LCD block diagram updated.	Anthony Chong	Celia Ki
1.0	24th Dec, 2013	All	-	Update version to rev1.0 as official version	Anthony Chong	Celia Ki
1.1	14th Jan, 2014	- 1 2 8	1	Revise feature list. Revise Electrical Charateristics. Revise pin assignment and pin description. Revise LCD section content.	Celia Ki	Danny Ho
1.2	12th Jun, 2014	2 8	-	Revise 48-pin pin assignment. Revise internal resistor ladder value.	Kennis To	Celia Ki
1.3	2nd Mar, 2015	1.2 1.3 1.9	-	Revise current consumption specification. Revise LVI specification. Revise oscillation specification.	Celia Ki	Kennis To
1.4	15th Jun, 2015	2	-	Correct I2C pin function label in LQFP48 pin 13 and pin 14	Celia Ki	Kennis To
1.5	29 th Mar, 2015	14.3		Revise the POD of LQFP64	Kennis To	Danny Ho
1.6	8th Aug 2016	1.9	-	Added crystal resonator recommendation	Patrick Li	Kennis To
1.7	11th Nov 2016	-	-	Revise package option	Patrick Li	Kennis To

Copyright Notice

Disclaimer

Dragonchip Ltd. assumes no responsibility for any errors contained herein.

Dragonchip Ltd.
TEL: (852) 2776-0111
FAX: (852) 2776-0996
http://www.dragonchip.com