DC6688F2SER

Super 1T 8051 Microcontroller

DC6688F2SER is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Power Down and Backup modes
- Power Monitor for low battery indicator
- Memory
  - 2000B Program Flash Memory
  - 16B Data Flash Memory
  - Security bit for read back protection
  - 64B SRAM
- IR generator by counter A with auto-reload function
- Built-in transistor for IR LED (I_{OL} = 300mA at V_{OL} = 0.5V)
- Four-level priority interrupt controller
- 16 bit-programmable I/O ports
- 16-bit Timers x 3
- Low Voltage Detection (LVD) for backup mode
- Low Voltage Indication (LVI)
- Maximum operating voltage: 3.6V
- Operating temperature: -40°C to +85°C
- Package type:
  - 20-pin TSSOP
  - 20-pin SSOP

Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B and C[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B and C[4]	+100	mA
Max. Power Dissipation	P_{max}	-	1.1W	W
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of I/O pin when configured to push-pull output high.
[2] It is measured as total for Ports A, B and C when configured to push-pull output high.
[3] It is measured for any one of I/O pin when configured to push-pull output low.
[4] It is measured as total for Ports A, B and C when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = V_{LVD1} to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input pins except XIN	0.7 V_{DD}	-	V_{DD}	V
	V_{IH2}	XIN	V_{DD} – 0.3	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input pins except XIN	0	-	0.3 V_{DD}	V
	V_{IL2}	XIN	0	-	0.3	V
Output High Voltage	V_{OH1}	All output pins except Port C1, V_{DD} = 3.0V, I_{OH} = - 10mA, T_A = 25°C	V_{DD} – 0.9	-	-	V
	V_{OH2}	Port C1, V_{DD} = 3.0V, I_{OH} = - 12mA, T_A = 25°C	V_{DD} – 0.9	-	-	V
Output Low Voltage	V_{OL1}	All output pins except Port C1, V_{DD} = 3.0V, I_{OL} = 10mA, T_A = 25°C	-	-	0.9	V
	V_{OL2}	Port C1, V_{DD} = 3.0V, I_{OL} = 14mA, T_A = 25°C	-	-	0.9	V
Output Low Current IR Transmit	$I_{OL(IRTX)}$	V_{OL} = 0.5V, IRDRV = 3, T_A = 25°C	-	300	-	mA
Input High Leakage Current	I_{LIH1}	All input pins except XIN, XOUT and ISPSEL, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH2}	XIN and XOUT, V_{IN} = V_{DD}	-	-	20	µA
	I_{LIH3}	ISPSEL, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input pins except XIN and XOUT, V_{IN} = 0	-	-	-1	µA
	I_{LIL2}	XIN and XOUT, V_{IN} = 0	-	-	-20	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{OUT} = V_{DD}	-	-	1	µA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output Low Leakage Current	I_{LOL}	All output pins, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{DD} = 3.0V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Pull-down Resistors	R_{PD}	V_{DD} = 3.0V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Supply Current Run Mode[1]	Idd(op)	f_{OSC} = 4MHz, V_{DD} = 3.0V, T_A = 25°C	-	3	6	mA
Supply Current Power Down Mode[2]	Idd(pd)	V_{DD} = 3.0V, T_A = 25°C	-	2	5	µA

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested if the condition is that:

a) Port A output open-drain.

b) Port B and C input enable pull-up resistor.

c) Port C1 output push-pull.

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Indicator	V_{LVI}	Default setting	1.9	2.1	2.35	V
		Program setting	2.0	2.3	2.6	V
Low Voltage Detect Level	V_{LVD1}		1.4	1.65	1.9	V

Remarks:

[1] $V_{LVD2} - V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage in Power Down Mode

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Power Down Mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 EEPROM Characteristics

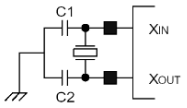
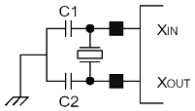
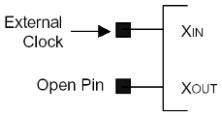
(V_{DD} = 2.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
EEPROM write time (1-byte)	t_{EEP_N}	XIN = 4MHz, Normal mode[1]	-	32	-	ms
	t_{EEP_F}	XIN = 4MHz, Fast mode[1]	-	22	-	ms

Remark:
[1] The mode of EEPROM is software configurable.

1.8 Oscillation Characteristics

(T_A = -40°C to +85°C)

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Crystal		CPU clock oscillation frequency	1	-	16.5	MHz
Ceramic		CPU clock oscillation frequency	1	-	16.5	MHz
External Clock		X_{IN} input frequency	1	-	16.5	MHz

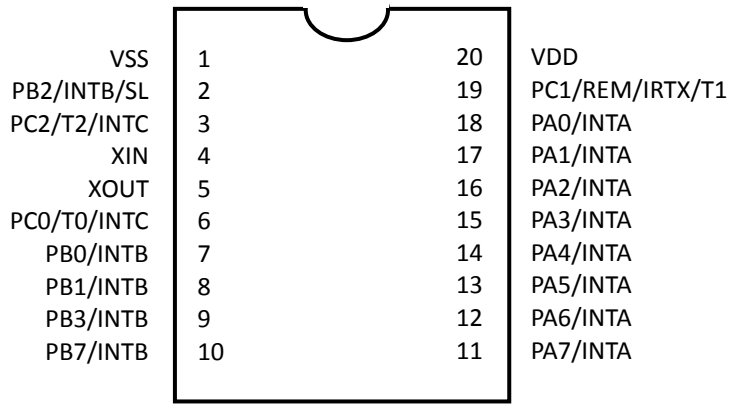
(T_A = -40°C to +85°C, V_{DD} = 3.0V)

Parameter	Conditions	Min	Typ	Max	Unit
Crystal	f_{OSC} > 1MHz Oscillation stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range	-	-	20	ms
Ceramic		-	-	10	ms
External Clock	X_{IN} input High and Low width(t_{XL}, t_{XH})	25	-	500	ns
Oscillator Stabilization Wait Time	tWAIT when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	tWAIT when released by an external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

Remarks:
[1] f_{osc} is the oscillator frequency.
[2] The duration of the oscillation stabilization time(tWAIT) when it is released from power down mode by PA or PB interrupt.

2 Pin Assignment

(TSSOP20/SSOP20)



TSSOP20 SSOP20	Pin Name	Symbol	Function
5	XOUT	XOUT	Crystal / oscillator output
4	XIN	XIN	Crystal / oscillator input
20	VDD	VDD	Power
1	VSS	VSS	Ground
18	PA0/INTA	PA0	Configurable input or output port
		INTA	Port interrupt input
17	PA1/INTA	PA1	Configurable input or output port
		INTA	Port interrupt input
16	PA2/INTA	PA2	Configurable input or output port
		INTA	Port interrupt input
15	PA3/INTA	PA3	Configurable input or output port
		INTA	Port interrupt input
14	PA4/INTA	PA4	Configurable input or output port
		INTA	Port interrupt input
13	PA5/INTA	PA5	Configurable input or output port
		INTA	Port interrupt input
12	PA6/INTA	PA6	Configurable input or output port
		INTA	Port interrupt input
11	PA7/INTA	PA7	Configurable input or output port
		INTA	Port interrupt input
7	PB0/INTB	PB0	Configurable input or output port
		INTB	Port interrupt input
8	PB1/INTB	PB1	Configurable input or output port
		INTB	Port interrupt input
2	PB2/INTB/SL	PB2	Input port
		INTB	Port interrupt input
		SL	SL (Single Line) communication signal
9	PB3/INTB	PB3	Configurable input or output port
		INTB	Port interrupt input
10	PB7/INTB	PB7	Configurable input or output port
		INTB	Port interrupt input

TSSOP20 SSOP20	Pin Name	Symbol	Function
6	PC0/T0/INTC	PC0	High current drive configurable I/O
		T0	Timer 0 external counter input
		INTC	Port interrupt input
19	PC1/REM/IRTX/T1	PC1	High current drive configurable I/0
		REM	Counter A carrier frequency output
		IRTX	IR transmit with built-in transistor
		T1	Timer 1 external counter input
3	PC2/T2/INTC	PC2	High current drive configurable I/0
		T2	Timer 2 external counter input
		INTC	Port interrupt input

3 Description

DC6688F2SER is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) and built-in transistor for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Memory

Memory comprises of the following elements, namely:

- 2000B Program Flash memory
- 16B Data Flash memory
- 64B Internal SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

4.1 Program & Data Flash Memory

A 2000 bytes on-chip program Flash and 16 bytes data Flash memory is provided for simple application. It can be programmed by In-System-Programming (ISP) method.
In addition, write protection signature is available to avoid writing accidentally.

4.2 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, etc. Some locations in the SFR address space are addressable as bits.

4.3 External Function Register (XFR)

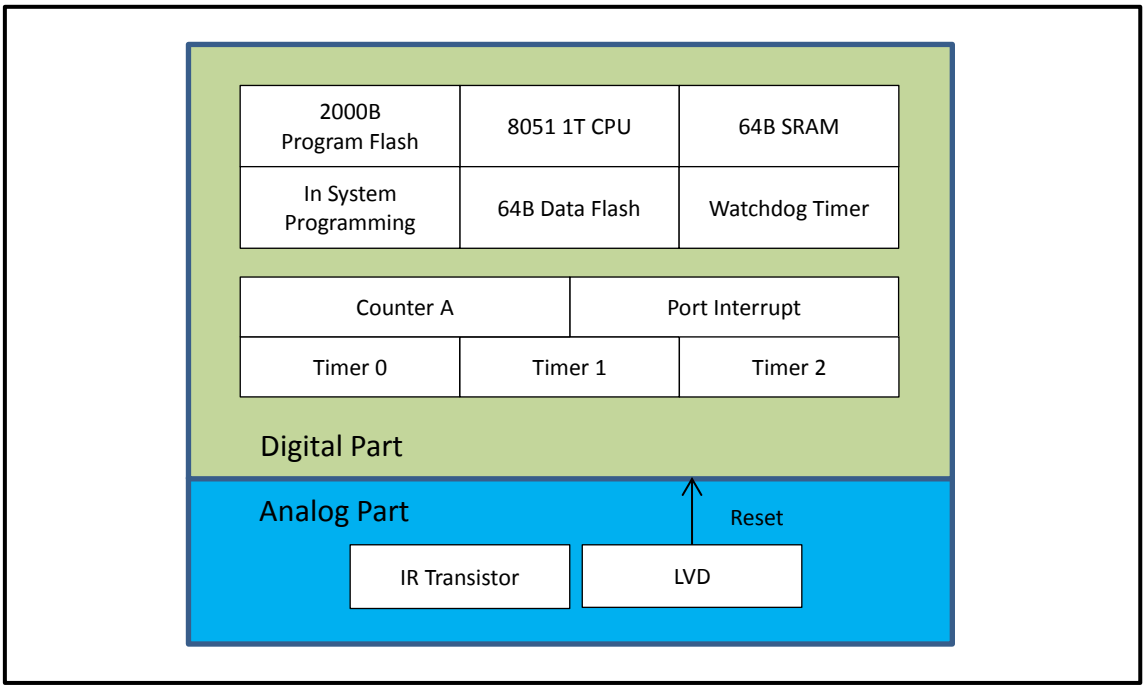
The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

5 Architecture

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

The block diagram is illustrated in the following figure.



6 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

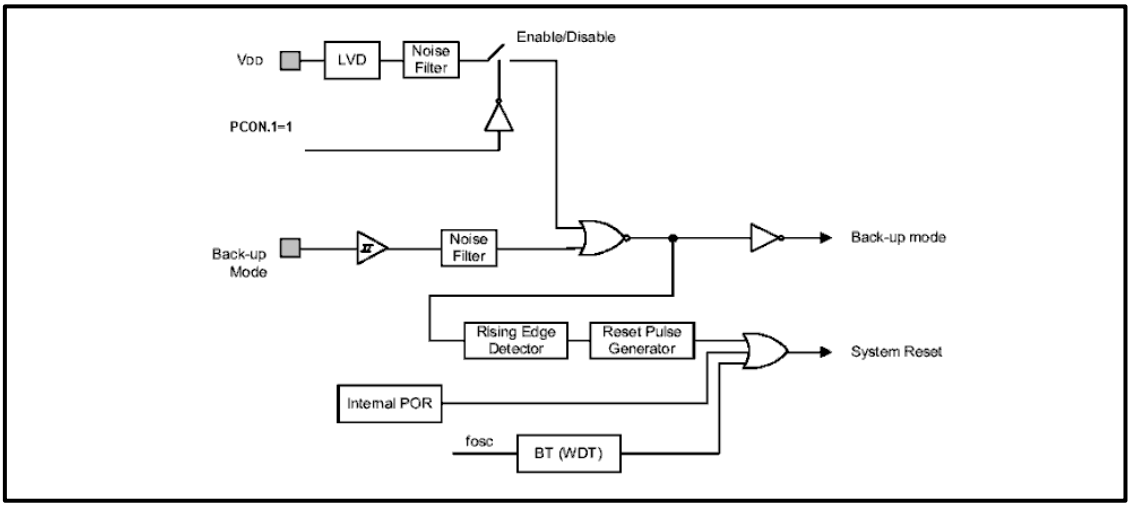
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

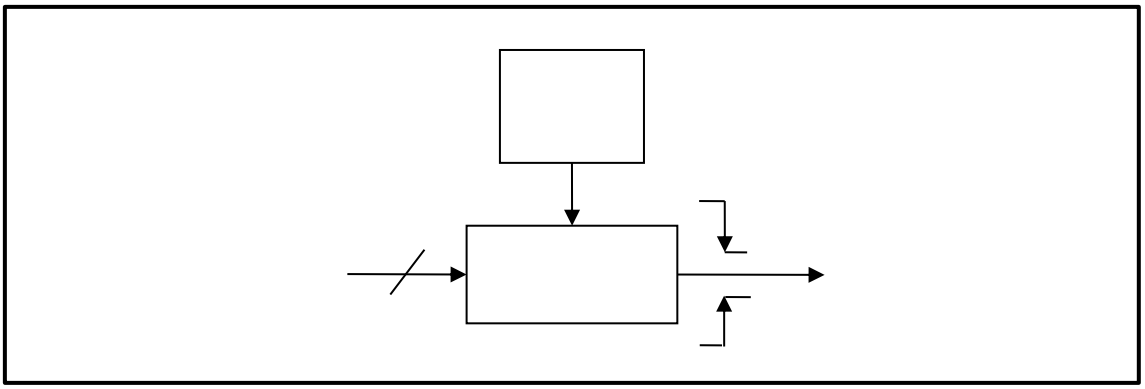
LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



8 I/O port

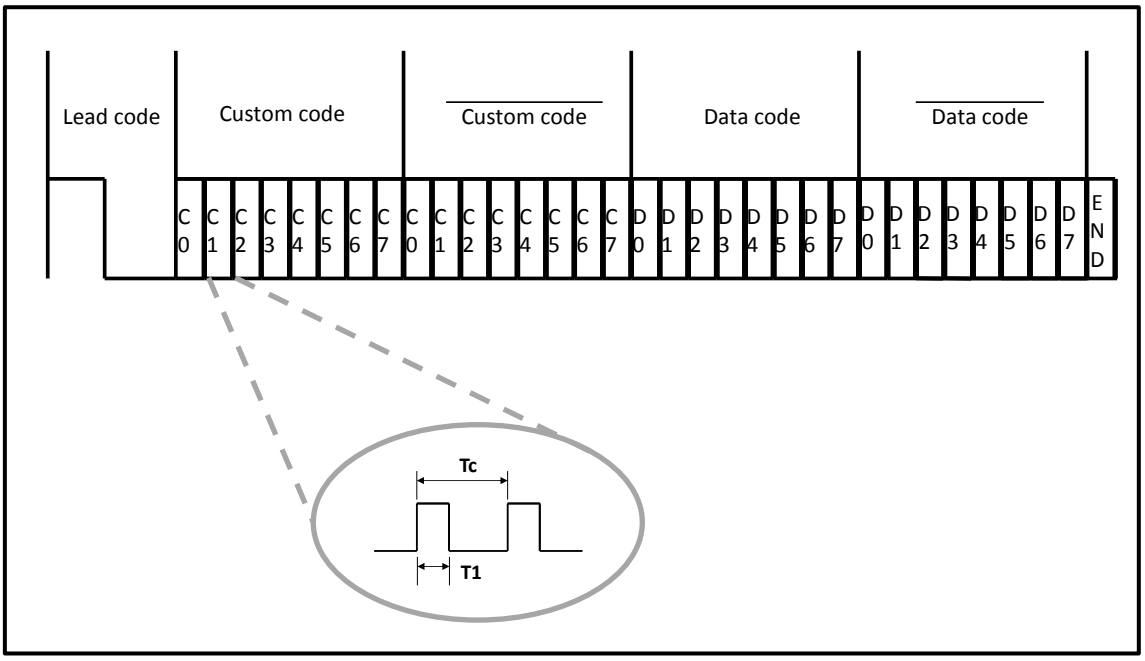
The 20-pin package has one 8-bit port (PA), one 4-bit port (PB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (XXXXXXXX). Port C is set to the value (00000XXX).

Port interrupt function is supported for port A, B and C. Pull-up and pull-down resistors are also included and could be assigned pin-by-pin by programming the pull-up or pull-down resistor enable register.



9 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



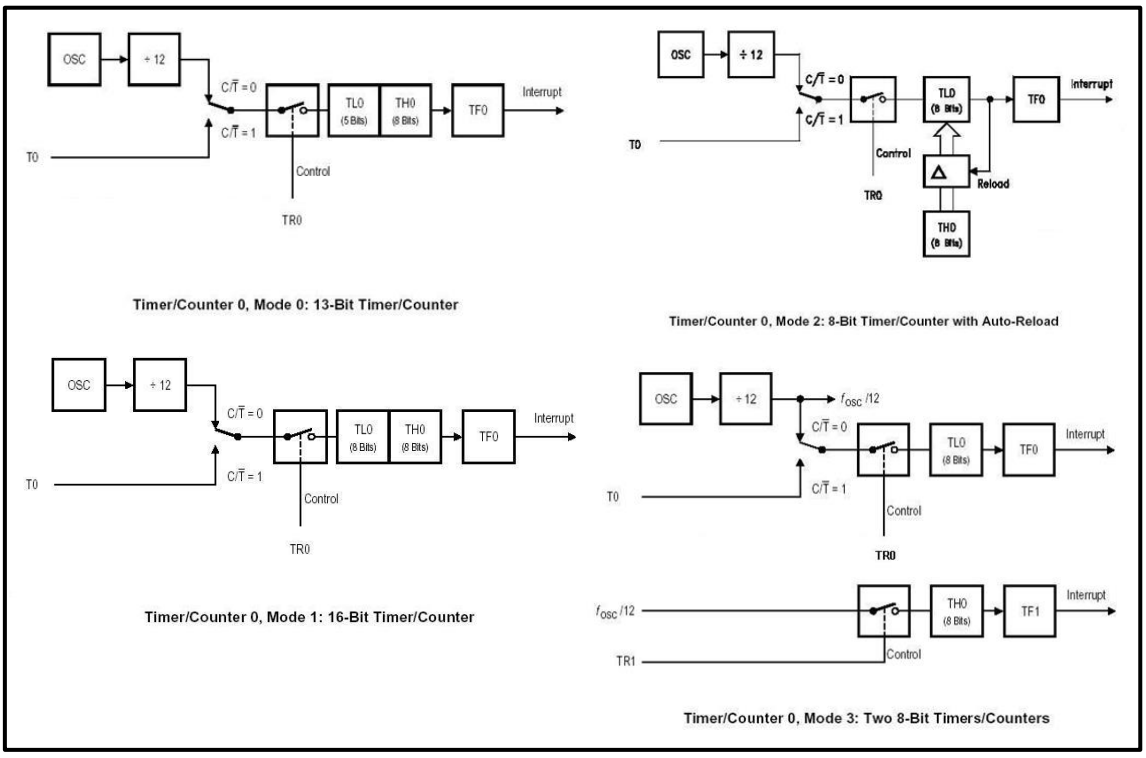
Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

10 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



11 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires only 3 wires to minimize the number of added components and board area impact.

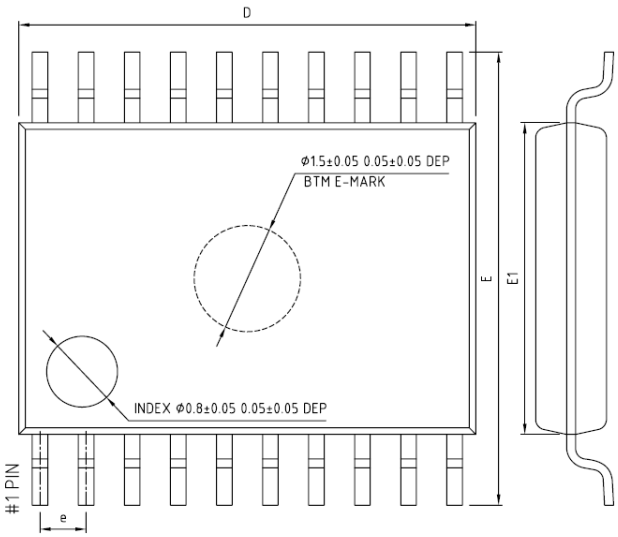
12 Ordering Information

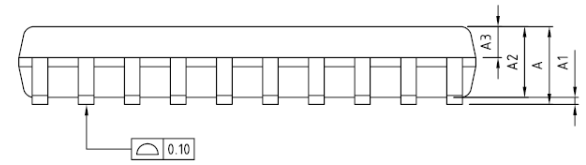
Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688F2SER	TSSOP20	2000B	16B	64B	16
DC6688F2SER-TR1	TSSOP20[1]	2000B	16B	64B	16
DC6688F2SERP	SSOP20	2000B	16B	64B	16
DC6688F2SERP-TR1	SSOP20[1]	2000B	16B	64B	16

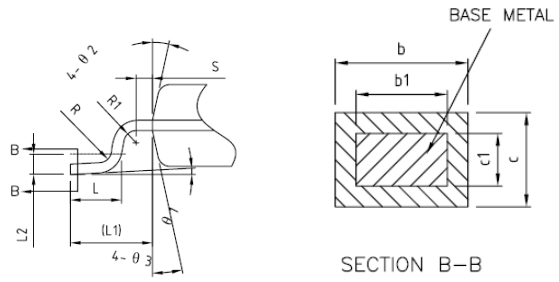
[1] Tape and reel packing.

13 Package Outlines

13.1 20-pin TSSOP







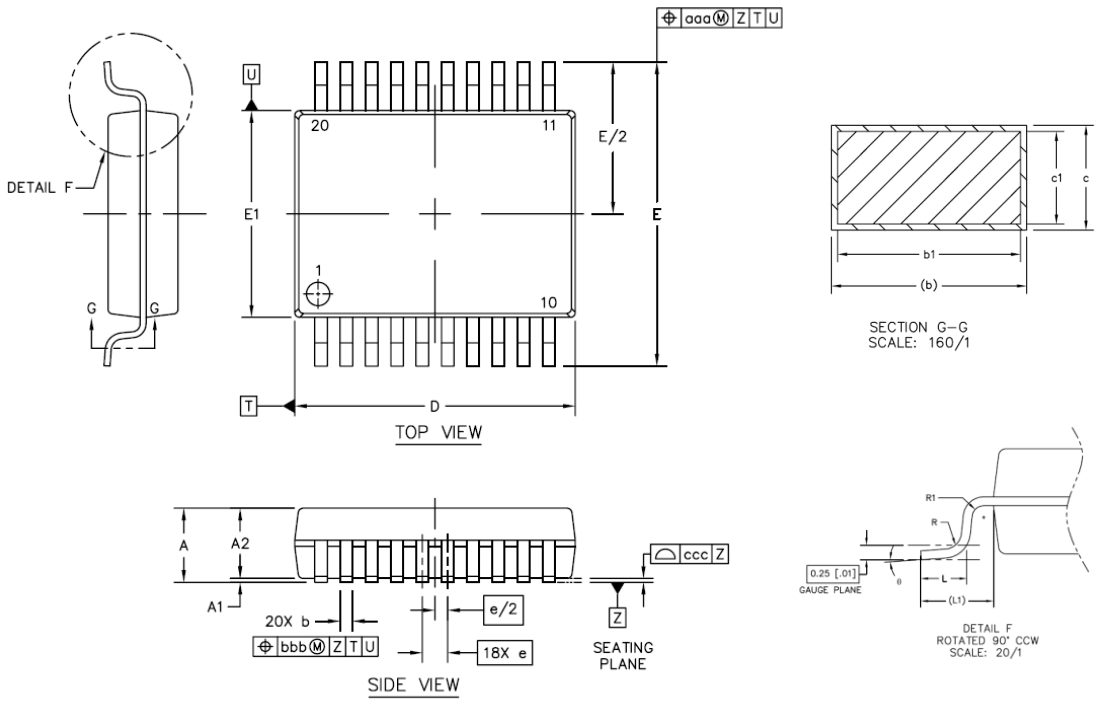
SECTION B–B

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

13.2 20-pin SSOP



	SYMBOL	MIN	NOM	MAX	MIN	NOM	MAX
TOTAL THICKNESS	A	1.8	---	1.99	.071	---	.078
STAND OFF	A1	0.05	---	0.14	.002	---	.006
MOLD THICKNESS	A2	1.75	---	1.85	.069	---	.073
LEAD WIDTH(PLATING)	b	0.25	---	0.38	.010	---	.015
LEAD WIDTH	b1	0.25	---	0.33	.010	---	.013
L/F THICKNESS(PLATING)	c	0.15	---	0.20	.006	---	.008
L/F THICKNESS	c1	0.10	---	0.16	.004	---	.006
BODY SIZE X	D	7.15	7.2	7.25	.281	.283	.285
BODY SIZE Y	E1	5.25	5.3	5.35	.207	.209	.211
	E	7.7	7.8	7.9	.303	.307	.311
LEAD PITCH	e	0.65 BSC			.026 BSC		
	L	0.63	---	0.95	.025	---	.037
FOOTPRINT	L1	1.25 REF			.049 REF		
	θ	0°	---	8°	0°	---	8°
	R	0.09	---	---	.004	---	---
	R1	0.09	---	---	.004	---	---
LEAD EDGE TOLERANCE	aaa	0.2			.008		
LEAD OFFSET	bbb	0.1			.004		
COPLANARITY	ccc	0.1			.004		

NOTES

1. DIMENSION D AND E1 DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON D IS 0.15mm(.006in) PER SIDE AND ON E1 IS 0.25mm(.010in) PER SIDE.

2. DIMENSION b DOES NOT INCLUDE DAM BAR PROTRUSION. ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13mm(.005in) TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.

14 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	2 Oct, 2013	All	-	New template	Celia Ki	Anthony Chong
1.1	9 Oct, 2013	4	-	Revise register description	Celia Ki	Anthony Chong
1.2	28 Oct, 2013	1.2	-	Revise IR transistor spec	Celia Ki	Anthony Chong
1.3	19 Mar, 2014	1, 2	-	Revise pin function description Revise operation temperature	Celia Ki	Anthony Chong
1.4	6 Jun, 2014	1.1	-	Add Max. power dissipation	Kennis To	Philip Hung
1.5	19 Sept, 2014	1.1		Add EEPROM characteristics	Philip Hung	Danny Ho
1.6	24 Aug, 2015	1.1		Revise LVI level	Kennis To	Eddy Cheung

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