DC6688F2SP

Long Distance IR 1-cell MCU with Built-in Voltage-Doubler

DC6688F2SP is an 8-bit Microcontroller Unit designed with built-in voltage doubler for single-battery operated applications. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Power Down and Backup modes
- Built-in voltage doubler to support single battery operated (1.1V-1.8V)
- Memory
  - 2000B Program Flash Memory
  - 16B Data Flash Memory
  - Security bit for read back protection
  - 64B SRAM
- Internal 4MHz oscillator
  - ± 1% accuracy from -20°C to +70°C , V_{CC} = 1.1V to 1.8V
- IR generator by counter A with auto-reload function
- Built-in transistor for IR LED (I_{OL} = 300mA at V_{OL} = 0.5V)
- Four-level priority interrupt controller
- 15 bit-programmable I/O ports
- 16-bit Timers x 3
- Low Voltage Detection (LVD)
- Low Voltage Indication (LVI)
- Maximum operating voltage: 1.8V
- Operating temperature: -40°C to +85°C
- Package type:
  - 16-pin SOP
  - 20-pin TSSOP

Quick look on Ordering Information

Table of Contents

1 Electrical Characteristics

1.1 Absolute Maximum Ratings

(T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{CC}	-	-0.3 to +1.9	V
Input Voltage	V_{IN}	-	-0.3 to V_{CC} + 0.3	V
Output Current High	I_{OH}	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B and C[2]	-60	mA
Output Current Low	I_{OL}	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B and C[4]	+100	mA
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

Remarks:
[1] It is measured for any one of I/O pin when configured to push-pull output high.
[2] It is measured as total for Ports A, B and C when configured to push-pull output high.
[3] It is measured for any one of I/O pin when configured to push-pull output low.
[4] It is measured as total for Ports A, B and C when configured to push-pull output low.

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{CC} = V_{LVD1} to 1.8 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{CC}	f_{OSC} = 4MHz	V_{LVD1}	-	1.8	V
Boosted Output Voltage	V_{out}	Run Mode	$2V_{cc}$– 0.2	-	-	V
		Power down mode	V_{cc}– 0.1	-	-	V
Input High Voltage	V_{IH}	All input pins	0.7 V_{out}	-	V_{out}	V
Input Low Voltage	V_{IL}	All input pins	0	-	0.3V_{out}	V
Output High Voltage	V_{OH1}	All output pins except Port C1, V_{CC}= 1.5V, I_{OH}= - 10mA, T_A= 25°C	V_{out}– 0.9	-	-	V
	V_{OH2}	Port C1, V_{CC} = 1.5V, I_{OH}= - 12mA, T_A = 25°C	V_{out}– 0.9	-	-	V
Output Low Voltage	V_{OL1}	All output pins except Port C1, V_{out}= 3.0V, I_{OL}= 10mA, T_A = 25°C	-	-	0.9	V
	V_{OL2}	Port C1, V_{out}= 3.0V, I_{OL}= 14mA, T_A = 25°C	-	-	0.9	V
Output Low Current IR Transmit	$I_{OL(IRTX)}$	V_{OL} = 0.5V, IRDRV = 3, T_A = 25°C	-	300	-	mA
Input High Leakage Current	I_{LIH}	All input pins, V_{IO} = V_{out}	-	-	1	µA
Input Low Leakage Current	I_{LIL}	All input pins, V_{IO} = 0	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output pins, V_{IO} = V_{out}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output pins, V_{IO} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{CC} = 1.5V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Pull-down Resistors	R_{PD}	V_{CC} = 1.5V, V_{IN} = 0 V; T_A = 25°C	75	150	300	kΩ
Run Mode Current[1]	Idd(op)	f_{OSC} = 4MHz, V_{CC}= 1.5V, T_A= 25°C	-	3	5	mA
Stop Mode Current[2]	Idd(pd)	V_{CC} = 1.5V, T_A = 25°C	-	4	7	µA

Remarks:
[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.
[2] Supply current is tested if the condition is that:
a) Port A output open-drain.
b) Port B and C input enable pull-up resistor.
c) Port C1 output push-pull.
d) Port D output push-pull.

1.3 Low Voltage Detect circuit Characteristics

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	100	-	mV
Low Voltage Detect Level	V_{LVD1}		0.9	1.0	1.1	V

Remarks:
[1] $V_{LVD2} – V_{LVD1} = \Delta V$

1.4 SRAM Data Retention Voltage in Power Down Mode

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	V_{DDDR}		1.0	-	1.8	V
Data Retention Supply Current	I_{DDDR}	V_{DDDR} = 1.0V Power Down Mode	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{CC} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

(V_{CC} = 1.5V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	-	100	-	Year
	t_{DRP2}	10k write/erase cycle	-	10	-	Year
	t_{DRP3}	100k write/erase cycle	-	1	-	Year

1.7 Oscillation Charateristics

Oscillator	Clock Circuit	Conditions	Min	Typ	Max	Unit
Internal 4MHz Oscillator	-	T_A = -20°C to +70°C , V_{CC} = 1.1V to 1.8V	-	-	± 1%	MHz

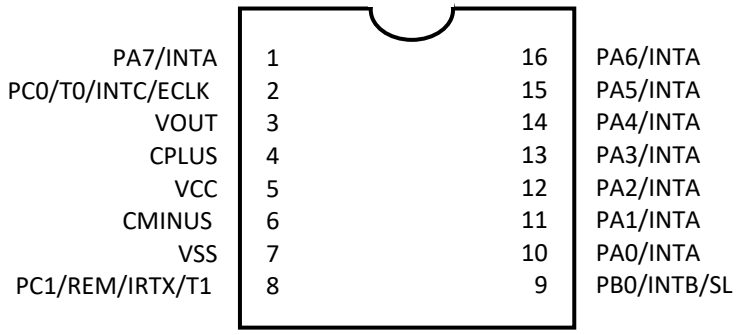
(T_A = -40°C to +85°C, V_{CC} = 1.5V)

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator Stabilization Wait Time	tWAIT when released by internal reset[1]	-	$2^{19}/f_{OSC}$	-	ms
	tWAIT when released by an external interrupt[2]	-	$2^{13}/f_{OSC}$	-	ms

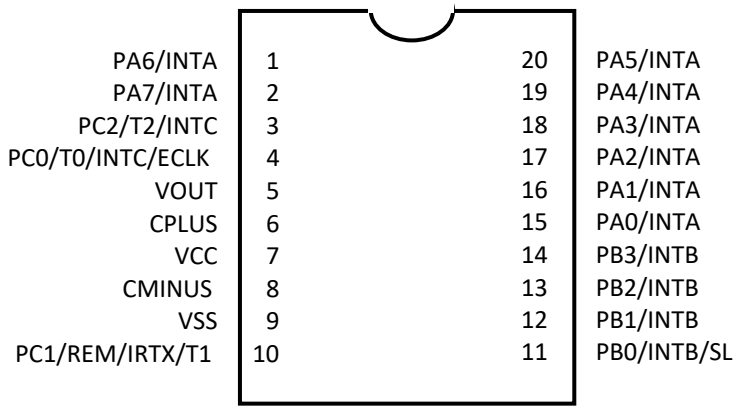
Remarks:
[1] f_{osc} is the oscillator frequency.
[2] The duration of the oscillation stabilization time(tWAIT) when it is released from power down mode by PA or PB interrupt.

2 Pin Assignment

(SOP16)



(TSSOP20)



SOP16	TSSOP20	Pin Name	Symbol	Function
5	7	VCC	VCC	Power
7	9	VSS	VSS	Ground
3	5	VOUT	VOUT	Voltage doubler output
4	6	CPLUS	CPLUS	10uF to CMINUS
6	8	CMINUS	CMINUS	10uF to CPLUS
10	15	PA0/INTA	PA0	Configurable input or output port
			INTA	Port interrupt input
11	16	PA1/INTA	PA1	Configurable input or output port
			INTA	Port interrupt input
12	17	PA2/INTA	PA2	Configurable input or output port
			INTA	Port interrupt input
13	18	PA3/INTA	PA3	Configurable input or output port
			INTA	Port interrupt input
14	19	PA4/INTA	PA4	Configurable input or output port
			INTA	Port interrupt input
15	20	PA5/INTA	PA5	Configurable input or output port
			INTA	Port interrupt input
16	1	PA6/INTA	PA6	Configurable input or output port

SOP16	TSSOP20	Pin Name	Symbol	Function
			INTA	Port interrupt input
1	2	PA7/INTA	PA7	Configurable input or output port
			INTA	Port interrupt input
9	11	PB0/INTB/SL	PB0	Configurable input or output port
			INTB	Port interrupt input
			SL	SL (Single Line) communication signal
-	12	PB1/INTB	PB1	Configurable input or output port
			INTB	Port interrupt input
-	13	PB2/INTB	PB2	Configurable input or output port
			INTB	Port interrupt input
-	14	PB3/INTB	PB3	Configurable input or output port
			INTB	Port interrupt input
2	4	PC0/T0/INTC/ECLK	PC0	High current drive configurable I/O
			T0	Timer 0 external counter input
			INTC	Port interrupt input
			ECLK	External clock for programming
8	10	PC1/REM/IRTX/T1	PC1	High current drive configurable I/0
			REM	Counter A carrier frequency output
			IRTX	IR transmit with built-in transistor
			T1	Timer 1 external counter input
-	3	PC2/T2/INTC	PC2	High current drive configurable I/0
			T2	Timer 2 external counter input
			INTC	Port interrupt input

3 Description

DC6688F2SP is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory. Internal RC oscillator is equipped, generating 4MHz machine clock without any external components.

The chip is equipped with dedicated carrier frequency generator (Counter A) and built-in transistor for IR remote controller application. It also included a voltage doubler which provides a boosted voltage for IR transmitter to increase its transmission distance. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

4 Architecture

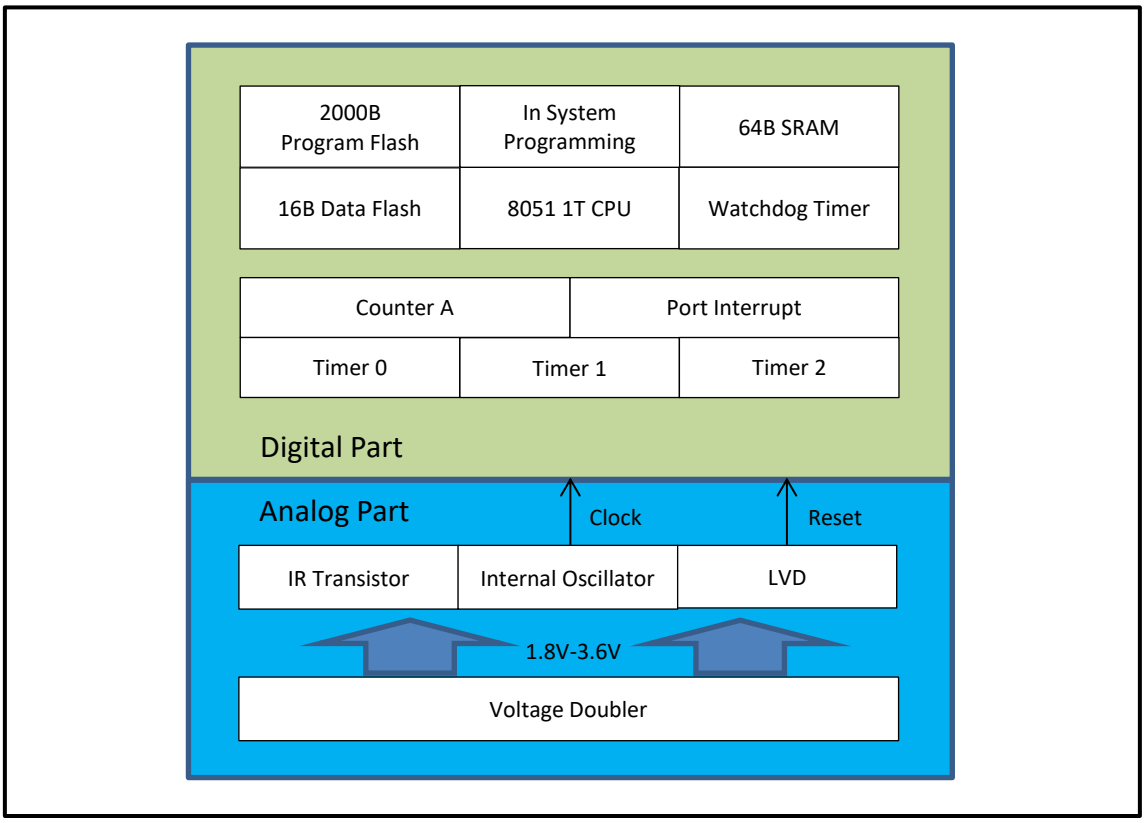
With the 1T 8051 8-bit MCS51 instruction compatible.CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models

and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

DC6688F2SP has internal RC oscillator built in. The oscillator is operated at 4MHz without external components. It supports trimming by In-System Programmer to ensure the oscillator within specification.

The block diagram is illustrated in the following figure.



5 Flash Memory

Memory comprises of the following elements, namely:

- 2000B Program Flash memory
- 16B Data Flash memory

A 2000 bytes on-chip program Flash and 16 bytes Data Flash memory is provided for simple application. Data flash memory can be programmed by In-System Programming (ISP) method with program Flash memory, and be read and written by application via EEPROM mannor. In addition, write protection signature is available to avoid writing accidentally.

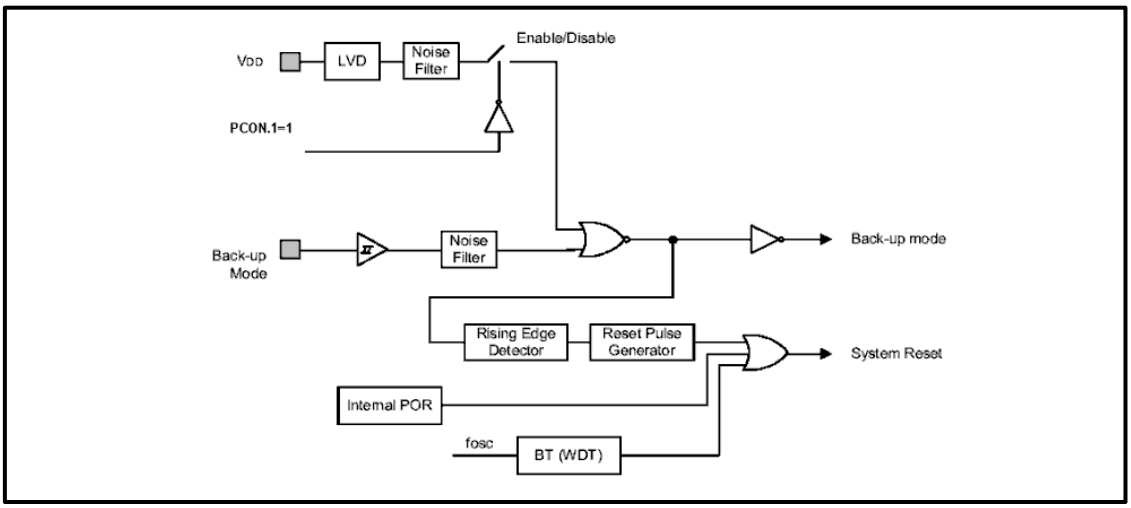
In addition, the program memory can be accessed by a simple external serial bus and therefore, In-System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life.

6 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{CC} by comparing the voltage at pin V_{CC} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{CC} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{CC} = V_{LVD1}".

On the other hand, system reset pulse is generated by the rising slope of V_{CC}. While the voltage at pin V_{CC} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{CC} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.

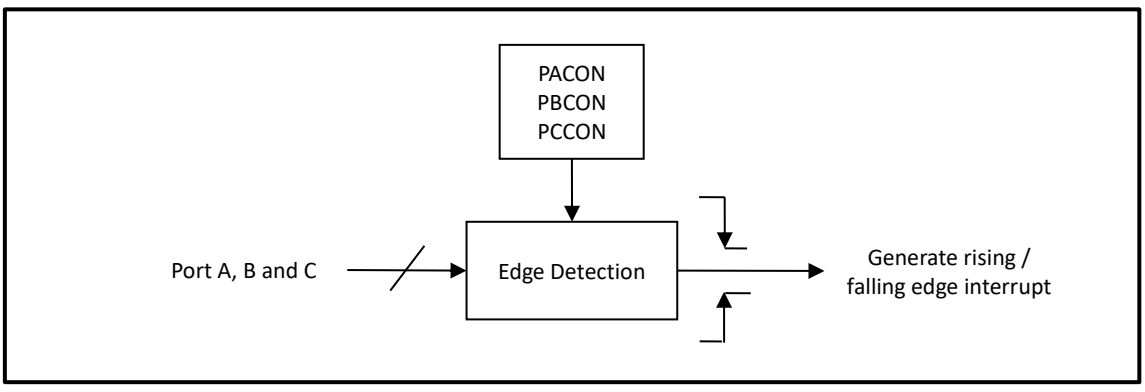


7 I/O port

The 16-pin package has one 8-bit port (PA), one 1-bit port (PB) and one 2-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

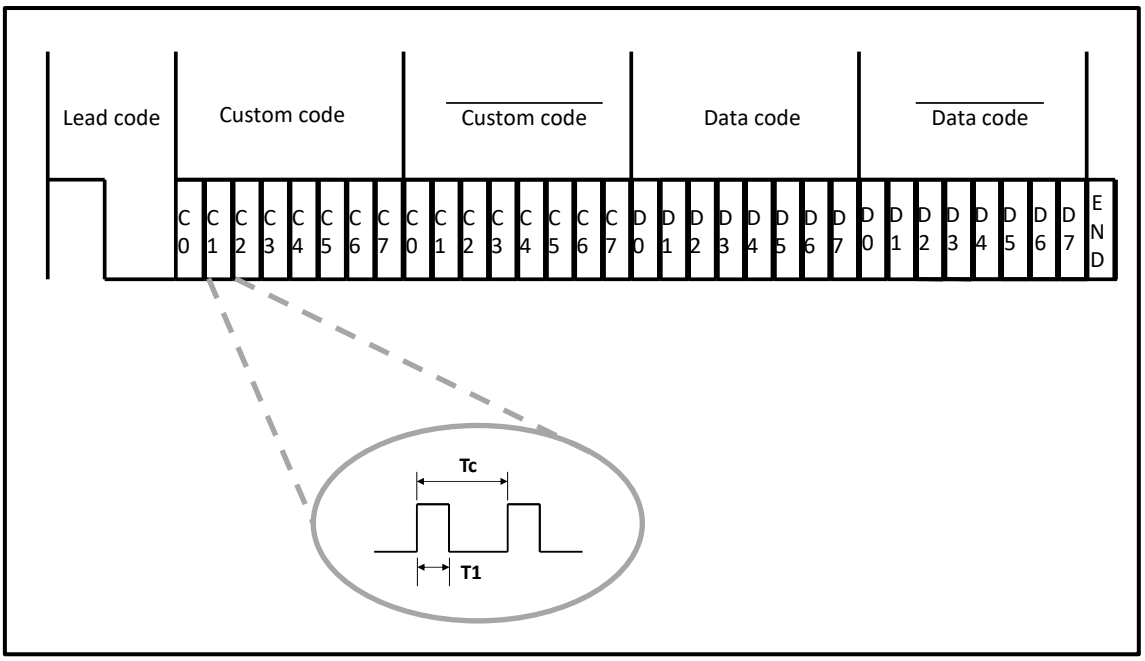
The 20-pin package has one 8-bit port (PA), one 4-bit port (PB) and one 3-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

Port interrupt function is supported for port A, B and C. Pull-up and pull-down resistors are also included and could be assigned pin-by-pin by programming the pull-up or pull-down resistor enable register.



8 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

9 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator

10 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 4 wires to minimize the number of added components and board area impact.

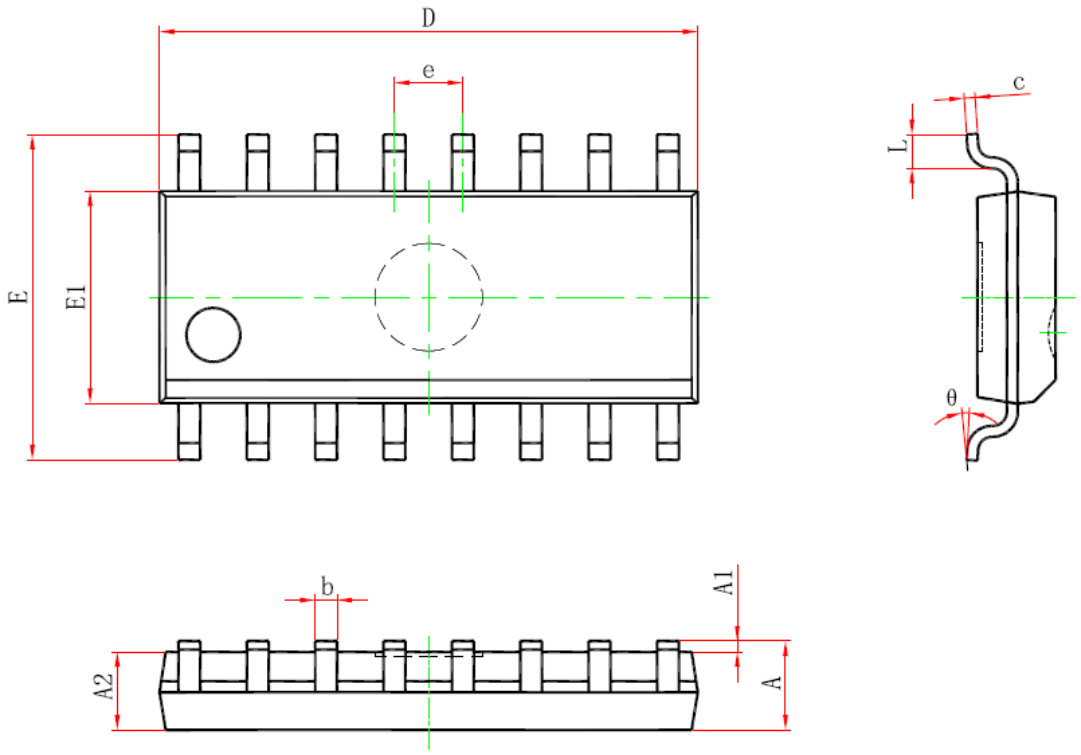
11 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688F2SPK	SOP16	2000B	16B	64B	11
DC6688F2SPK-TR1	SOP16[1]	2000B	16B	64B	11
DC6688F2SPN	TSSOP20	2000B	16B	64B	15
DC6688F2SPN-TR1	TSSOP20[1]	2000B	16B	64B	15

[1] Tape and reel packing.

12 Package Outlines

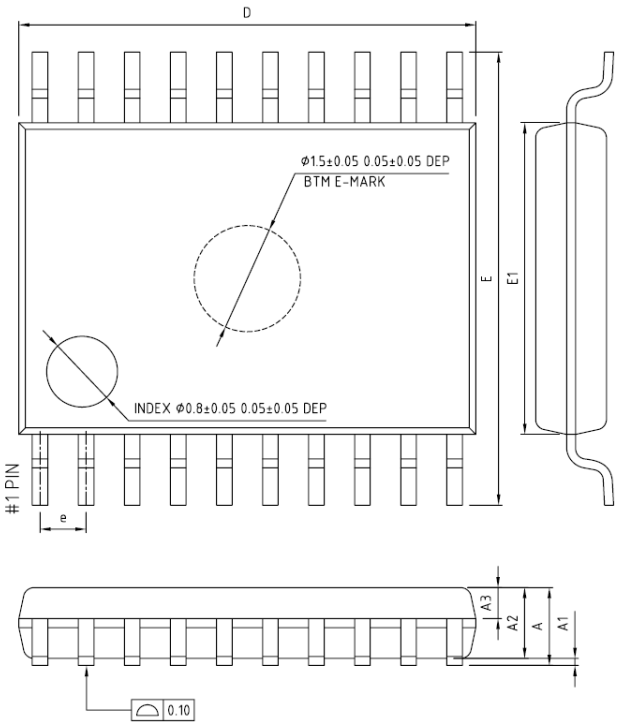
12.1 16-pin SOP

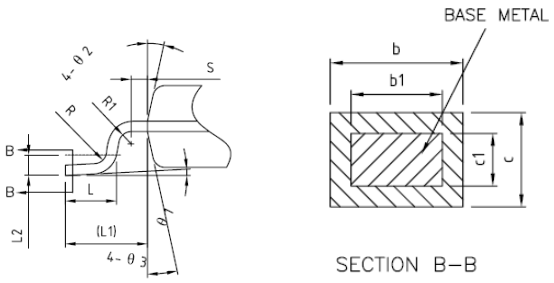


NOTES:
ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	**Max**	**Min**	**Max**
A	---	1.750	---	0.069
A1	0.100	0.250	0.004	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

12.2 20-pin TSSOP





NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 AC
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.90	1.00	1.05
A3	0.34	0.44	0.54
b	0.20	–	0.28
b1	0.20	0.22	0.24
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	6.40	6.50	6.60
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
e		0.65BSC	
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	10°	12°	14°
θ3	10°	12°	14°

13 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
0.1	15 Dec, 2014	All	-	Initial Release	Kennis To	Celia Ki
0.2	19 Dec, 2014	All		Correct typo	Kennis To	Celia Ki
0.3	19 Dec, 2014	12		Revise the part number	Kennis To	Eddy Cheung
0.4	19 Dec, 2014	12		Revise the part number	Kennis To	Eddy Cheung
0.5	5 Sep, 2016			Format adjustment	Patrick Li	Patrick Chan
0.6	15 Jun 2017	All		Changed F2P to F2SPN; Modified description	Patrick Chan	Eddy Cheung
1.0	11 Sep 2017	2, 7, 11, 12		Add DC6688F2SPK	Kennis To	Danny Ho
1.1	11 Sep 2017	All		Correct datasheet name to DC6688F2SP	Kennis To	Danny Ho
1.2	4 Oct, 2018	-	1	Modified title to “Long Distance IR 1-cell MCU with Built-in Voltage-Doubler”	Patrick Chan	Fred Law

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