



# DC6688F2STR

## Super 1T 8051 Microcontroller

DC6688F2STR is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory.

### Features

- ◆ High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- ◆ Power Down and Backup modes
- ◆ Memory
  - ◇ 2000B Program Flash Memory
  - ◇ 16B Data Flash Memory
  - ◇ Security bit for read back protection
  - ◇ 64B SRAM
- ◆ Internal 4MHz oscillator
  - ◇  $\pm 1\%$  accuracy from  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{\text{DD}} = 1.8\text{V}$  to  $3.6\text{V}$
- ◆ IR generator by counter A with auto-reload function
- ◆ Built-in transistor for IR LED ( $I_{\text{OL}} = 300\text{mA}$  at  $V_{\text{OL}} = 0.5\text{V}$ )
- ◆ Four-level priority interrupt controller
- ◆ 18 bit-programmable I/O ports
- ◆ 16-bit Timers x 3
- ◆ Low Voltage Detection (LVD)
- ◆ Low Voltage Indication (LVI)
- ◆ Maximum operating voltage: 3.6V
- ◆ Operating temperature:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$
- ◆ Package type:
  - ◇ 20-pin TSSOP
  - ◇ 16-pin TSSOP
  - ◇ 16-pin SOP

Quick look on [Ordering Information](#)

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## 1 Electrical Characteristics

### 1.1 Absolute Maximum Ratings

( $T_A = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	$V_{DD}$	-	-0.3 to +3.8	V
Input Voltage	$V_{IN}$	-	-0.3 to $V_{DD} + 0.3$	V
Output Current High	$I_{OH}$	One I/O pin active[1]	-18	mA
		Total pin current for ports A,B and C[2]	-60	mA
Output Current Low	$I_{OL}$	One I/O pin active[3]	+30	mA
		Total pin current for ports A,B and C[4]	+100	mA
Operating Temperature	$T_A$	-	-40 to +85	$^\circ\text{C}$
Storage Temperature	$T_{STG}$	-	-65 to +150	$^\circ\text{C}$

Remarks:

- [1] It is measured for any one of I/O pin when configured to push-pull output high.  
 [2] It is measured as total for Ports A, B and C when configured to push-pull output high.  
 [3] It is measured for any one of I/O pin when configured to push-pull output low.  
 [4] It is measured as total for Ports A, B and C when configured to push-pull output low.

### 1.2 DC Electrical Characteristics

( $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{DD} = V_{LVD1}$  to 3.6 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	$V_{DD}$	$f_{OSC} = 4\text{MHz}$	$V_{LVD1}$	-	3.6	V
Input High Voltage	$V_{IH}$	All input pins	$0.7 V_{DD}$	-	$V_{DD}$	V
Input Low Voltage	$V_{IL}$	All input pins	0	-	$0.3 V_{DD}$	V
Output High Voltage	$V_{OH1}$	All output pins except Port C1, $V_{DD} = 3.0\text{V}$ , $I_{OH} = -10\text{mA}$ , $T_A = 25^\circ\text{C}$	$V_{DD} - 0.9$	-	-	V
	$V_{OH2}$	Port C1, $V_{DD} = 3.0\text{V}$ , $I_{OH} = -12\text{mA}$ , $T_A = 25^\circ\text{C}$	$V_{DD} - 0.9$	-	-	V
Output Low Voltage	$V_{OL1}$	All output pins except Port C1, $V_{DD} = 3.0\text{V}$ , $I_{OL} = 10\text{mA}$ , $T_A = 25^\circ\text{C}$	-	-	0.9	V
	$V_{OL2}$	Port C1, $V_{DD} = 3.0\text{V}$ , $I_{OL} = 14\text{mA}$ , $T_A = 25^\circ\text{C}$	-	-	0.9	V
Output Low Current IR Transmit	$I_{OL(IRTX)}$	$V_{OL} = 0.5\text{V}$ , $IRDRV = 3$ , $T_A = 25^\circ\text{C}$	-	300	-	mA
Input High Leakage Current	$I_{LIH}$	All input pins, $V_{IN} = V_{DD}$	-	-	1	$\mu\text{A}$
Input Low Leakage Current	$I_{LIL}$	All input pins, $V_{IN} = 0$	-	-	-1	$\mu\text{A}$
Output High Leakage Current	$I_{LOH}$	All output pins, $V_{OUT} = V_{DD}$	-	-	1	$\mu\text{A}$
Output Low Leakage Current	$I_{LOL}$	All output pins, $V_{OUT} = 0\text{V}$	-	-	-1	$\mu\text{A}$
Pull-up Resistors	$R_{PU}$	$V_{DD} = 3.0\text{V}$ , $V_{IN} = 0\text{V}$ ; $T_A = 25^\circ\text{C}$	75	150	300	k $\Omega$
Pull-down Resistors	$R_{PD}$	$V_{DD} = 3.0\text{V}$ , $V_{IN} = 0\text{V}$ ; $T_A = 25^\circ\text{C}$	75	150	300	k $\Omega$
Supply Current Run Mode[1]	$I_{dd(op)}$	$f_{OSC} = 4\text{MHz}$ , $V_{DD} = 3.0\text{V}$ , $T_A = 25^\circ\text{C}$	-	1.5	3	mA
Supply Current Power Down Mode[2]	$I_{dd(pd)}$	$V_{DD} = 3.0\text{V}$ , $T_A = 25^\circ\text{C}$	-	2	5	$\mu\text{A}$

Remarks:

[1] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[2] Supply current is tested if the condition is that:

- a) Port A output open-drain.
- b) Port B and C input enable pull-up resistor.
- c) Port C1 output push-pull.
- d) Port D output push-pull.

### 1.3 Low Voltage Detect circuit Characteristics

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	$\Delta V[1]$		-	100	-	mV
Low Voltage Indicator	$V_{LVI}$	Program setting	1.65	1.8	1.95	V
		Default setting	2.0	2.15	2.3	V
		Program setting	2.35	2.5	2.65	V
		Program setting	2.65	2.8	2.95	V
Low Voltage Detect Level	$V_{LVD1}$		1.4	1.5	1.6	V

Remarks:

[1]  $V_{LVD2} - V_{LVD1} = \Delta V$

### 1.4 SRAM Data Retention Voltage in Power Down Mode

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Supply Voltage	$V_{DDDR}$		1.0	-	3.6	V
Data Retention Supply Current	$I_{DDDR}$	$V_{DDDR} = 1.0\text{V}$ Power Down Mode	-	-	1	$\mu\text{A}$

### 1.5 Input/Output Capacitance

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 0\text{V}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	$C_{IN}$	$f = 1\text{MHz}$ ; unmeasured pins are connected to $V_{SS}$	-	-	10	$\mu\text{F}$
Output Capacitance	$C_{OUT}$					
I/O Capacitance	$C_{IO}$					

### 1.6 Flash Memory Data Retention

( $V_{DD} = 2.5\text{V}$ ,  $T_A = 25^{\circ}\text{C}$ )

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	$t_{DRP1}$	1 write/erase cycle	-	100	-	Year
	$t_{DRP2}$	10k write/erase cycle	-	10	-	Year
	$t_{DRP3}$	100k write/erase cycle	-	1	-	Year

### 1.7 Oscillation Characteristics

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Internal 4MHz Oscillator	$f_{OSC}$	$T_A = -20^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ , $V_{DD} = 1.8\text{V}$ to $3.6\text{V}$	-	-	$\pm 1\%$	MHz

Oscillator	Symbol	Conditions	Min	Typ	Max	Unit
Internal low-frequency oscillator clock frequency	$f_{LF}$	$T_A = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ , $V_{DD} = V_{LVD1}$ to 3.6V	25	50	75	kHz

( $T_A = -40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ ,  $V_{DD} = 3.0\text{V}$ )

Parameter	Conditions	Min	Typ	Max	Unit
Oscillator Stabilization Wait Time	tWAIT when released by internal reset[1]	-	$2^{19}/f_{osc}$	-	ms
	tWAIT when released by an external interrupt[2]	-	$2^{13}/f_{osc}$	-	ms

Remarks:

[1]  $f_{osc}$  is the oscillator frequency.

[2] The duration of the oscillation stabilization time(tWAIT) when it is released from power down mode by PA or PB interrupt.

## 2 Pin Assignment

(SOP16/TSSOP16)

VSS	1	16	VDD
PB2/INTB	2	15	PC1/REM/IRTX/T1
PC2/T2/INTC	3	14	PA2/INTA
PC4/INTC	4	13	PA3/INTA
PC3/INTC	5	12	PA4/INTA
PC0/T0/INTC/ECLK/T2EX	6	11	PA5/INTA
PB0/INTB/SL	7	10	PA6/INTA
PB1/INTB	8	9	PA7/INTA

(TSSOP20)

VSS	1	20	VDD
PB2/INTB	2	19	PC1/REM/IRTX/T1
PC2/T2/INTC	3	18	PA0/INTA
PC4/INTC	4	17	PA1/INTA
PC3/INTC	5	16	PA2/INTA
PC0/T0/INTC/ECLK/T2EX	6	15	PA3/INTA
PB0/INTB/SL	7	14	PA4/INTA
PB1/INTB	8	13	PA5/INTA
PB3/INTB	9	12	PA6/INTA
PB7/INTB	10	11	PA7/INTA

TSSOP16	TSSOP20	Pin Name	Symbol	Function
16	20	VDD	VDD	Power
1	1	VSS	VSS	Ground
-	18	PA0/INTA	PA0	Configurable input or output port
-	18	PA0/INTA	INTA	Port interrupt input
-	17	PA1/INTA	PA1	Configurable input or output port
-	17	PA1/INTA	INTA	Port interrupt input
14	16	PA2/INTA	PA2	Configurable input or output port
14	16	PA2/INTA	INTA	Port interrupt input
13	15	PA3/INTA	PA3	Configurable input or output port
13	15	PA3/INTA	INTA	Port interrupt input
12	14	PA4/INTA	PA4	Configurable input or output port
12	14	PA4/INTA	INTA	Port interrupt input
11	13	PA5/INTA	PA5	Configurable input or output port
11	13	PA5/INTA	INTA	Port interrupt input
10	12	PA6/INTA	PA6	Configurable input or output port
10	12	PA6/INTA	INTA	Port interrupt input
9	11	PA7/INTA	PA7	Configurable input or output port
9	11	PA7/INTA	INTA	Port interrupt input

TSSOP16	TSSOP20	Pin Name	Symbol	Function
7	7	PB0/INTB/SL	PB0	Configurable input or output port
			INTB	Port interrupt input
			SL	SL (Single Line) communication signal
8	8	PB1/INTB	PB1	Configurable input or output port
			INTB	Port interrupt input
2	2	PB2/INTB	PB2	Configurable input or output port
			INTB	Port interrupt input
-	9	PB3/INTB	PB3	Configurable input or output port
			INTB	Port interrupt input
-	10	PB7/INTB	PB7	Configurable input or output port
			INTB	Port interrupt input
6	6	PC0/T0/INTC/ECLK/T2 EX	PC0	High current drive configurable I/O
			T0	Timer 0 external counter input
			INTC	Port interrupt input
			ECLK	External clock for programming
			T2EX	Timer 2 capture-reload trigger / up down count
15	19	PC1/REM/IRTX/T1	PC1	High current drive configurable I/O
			REM	Counter A carrier frequency output
			IRTX	IR transmit with built-in transistor
			T1	Timer 1 external counter input
3	3	PC2/T2/INTC	PC2	High current drive configurable I/O
			T2	Timer 2 external counter input
			INTC	Port interrupt input
5	5	PC3/INTC	PC3	High current drive configurable I/O
			INTC	Port interrupt input
4	4	PC4/INTC	PC3	High current drive configurable I/O
			INTC	Port interrupt input

### 3 Description

DC6688F2STR is an 8-bit Microcontroller Unit designed with low voltage embedded Flash memory. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory. Internal RC oscillator is equipped, generating 4MHz machine clock without any external components.

With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded as program or data memory. User can design the chips for different kind of models and applications without worrying problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after product assembly.

The chip is equipped with dedicated carrier frequency generator (Counter A) and built-in transistor for IR remote controller application. Power management circuits such as the idle mode, power down mode and back up mode, working with the low voltage detection circuit, make the chips perfect for battery-operated, handheld devices.

## 4 Memory

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Memory comprises of the following elements, namely:

- ◆ 2000B Program Flash memory
- ◆ 16B Data Flash memory
- ◆ 64B Internal SRAM
- ◆ 128B Special function register (SFR)
- ◆ 256B External special function register (XFR)

### 4.1 Program & Data Flash Memory

A 2000 bytes on-chip program Flash and 16 bytes data Flash memory is provided for simple application. It can be programmed by In-System-Programming (ISP) method.

In addition, write protection signature is available to avoid writing accidentally.

### 4.2 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, etc. Some locations in the SFR address space are addressable as bits.

### 4.3 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

## 5 Architecture

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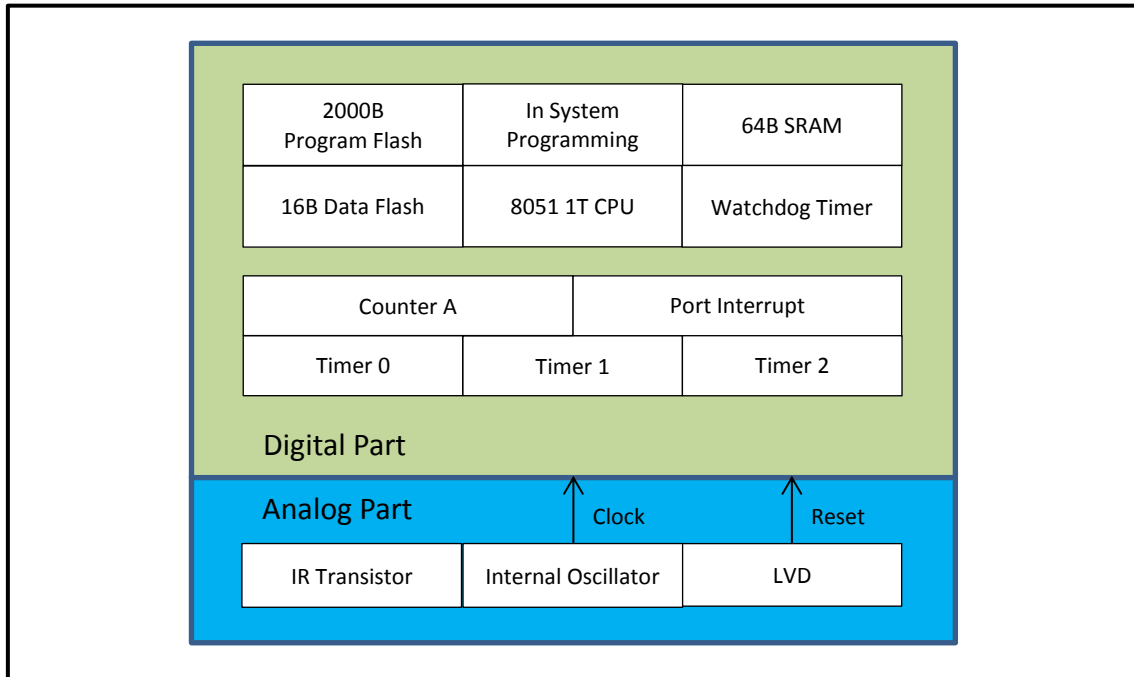
With the 1T 8051 8-bit CPU, instruction execution time is just 125ns at 8Mhz operating frequency. Such high performance CPU provides an option for system design to use slow system clock in order to lower the overall operating power consumption which is important to all battery-operated products.

Highly reliable, low voltage operated Flash memory block is designed and embedded into the chips for both program memory and user data memory. User can design the chips for different kind of models and applications without worry problems about long mask ROM cycle time, inventory burden, end customers rescheduling and product end of life. In addition, the program memory can be accessed by a simple external serial bus and therefore, In System Programming (ISP) can be implemented into the target system easily where late programming, upgrade or even model change are possible even after production assemble. The built-in data Flash memory can be used to store real time user data and the function is just same as EEPROM.

DC6688F2STR has internal RC oscillator built in. The oscillator is operated at 4MHz without external components. It supports trimming by In-System Programmer to ensure the oscillator within specification.

The block diagram is illustrated in the following figure.





## 6 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

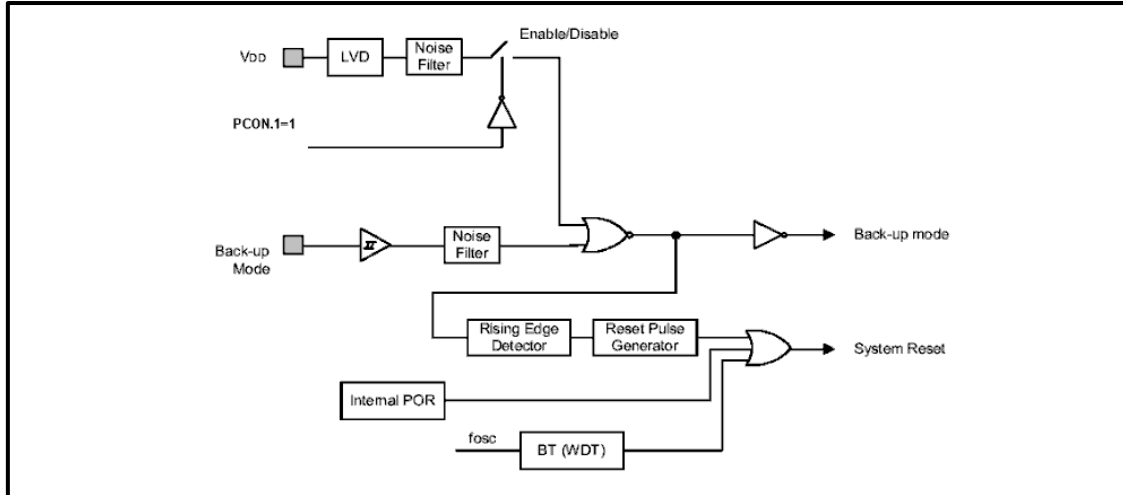
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

## 7 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of  $V_{DD}$  by comparing the voltage at pin  $V_{DD}$  with reference voltage,  $V_{LVD1}$  (Low Voltage Detect Voltage Level 1). Whenever the voltage at  $V_{DD}$  is falling down and passing  $V_{LVD1}$ , the IC goes into back-up mode at the moment " $V_{DD} = V_{LVD1}$ ".

On the other hand, system reset pulse is generated by the rising slope of  $V_{DD}$ . While the voltage at pin  $V_{DD}$  is rising up and passing  $V_{LVD2}$  (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment " $V_{DD} \geq V_{LVD2}$ ".

LVD provides a hysteresis ( $V_{LVD2} - V_{LVD1}$ ) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.

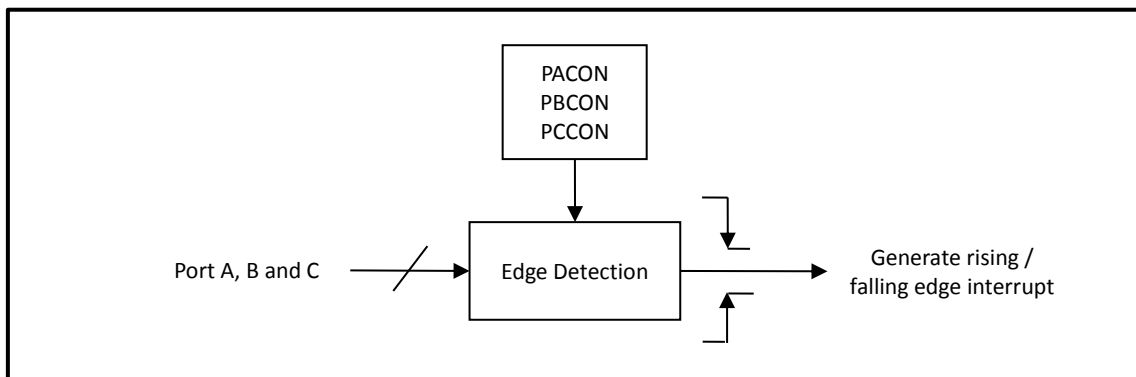


## 8 I/O port

The 20-pin package has one 8-bit port (PA), one 5-bit port (PB) and one 5-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

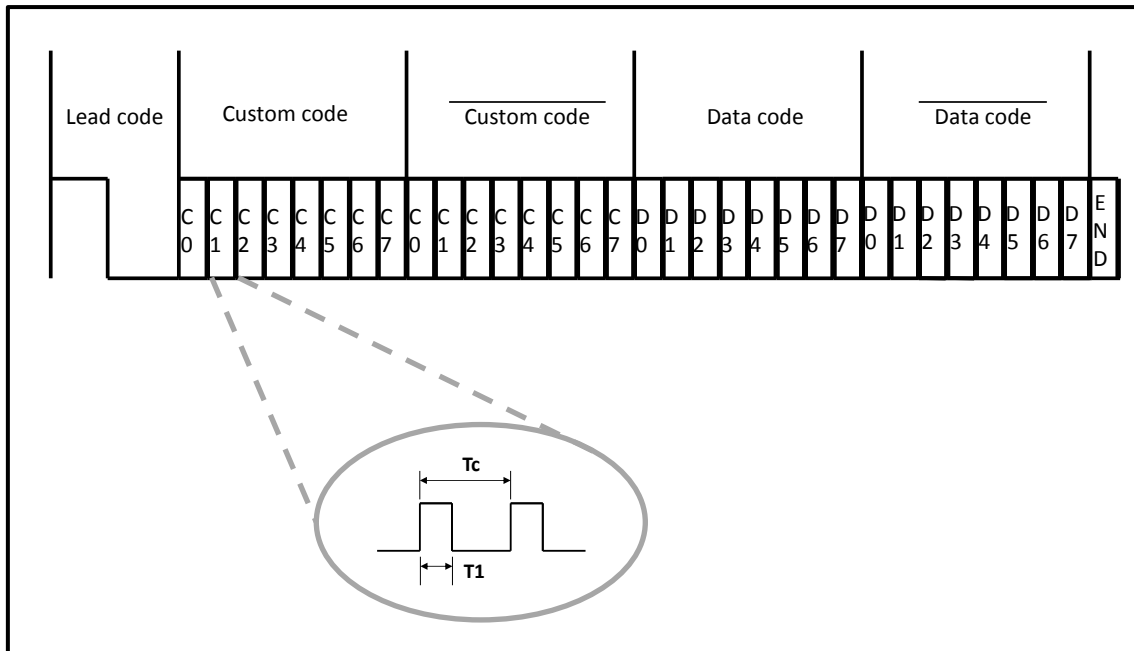
The 16-pin package has one 6-bit port (PA), one 3-bit port (PB) and one 5-bit port (PORTC). All ports are latches used to drive the bi-directional I/O lines.

Port interrupt function is supported for port A, B and C. Pull-up and pull-down resistors are also included and could be assigned pin-by-pin by programming the pull-up or pull-down resistor enable register.



## 9 Counter A (IR Carrier Frequency Generator)

Counter A is a 16-bit counter. It can be used to generate the carrier frequency of remote controller.



Counter A can also be used as PWM counter with two 8-bit data registers. It supports 5 – 8 bit mode selection and 1 – 128 clock division selection.

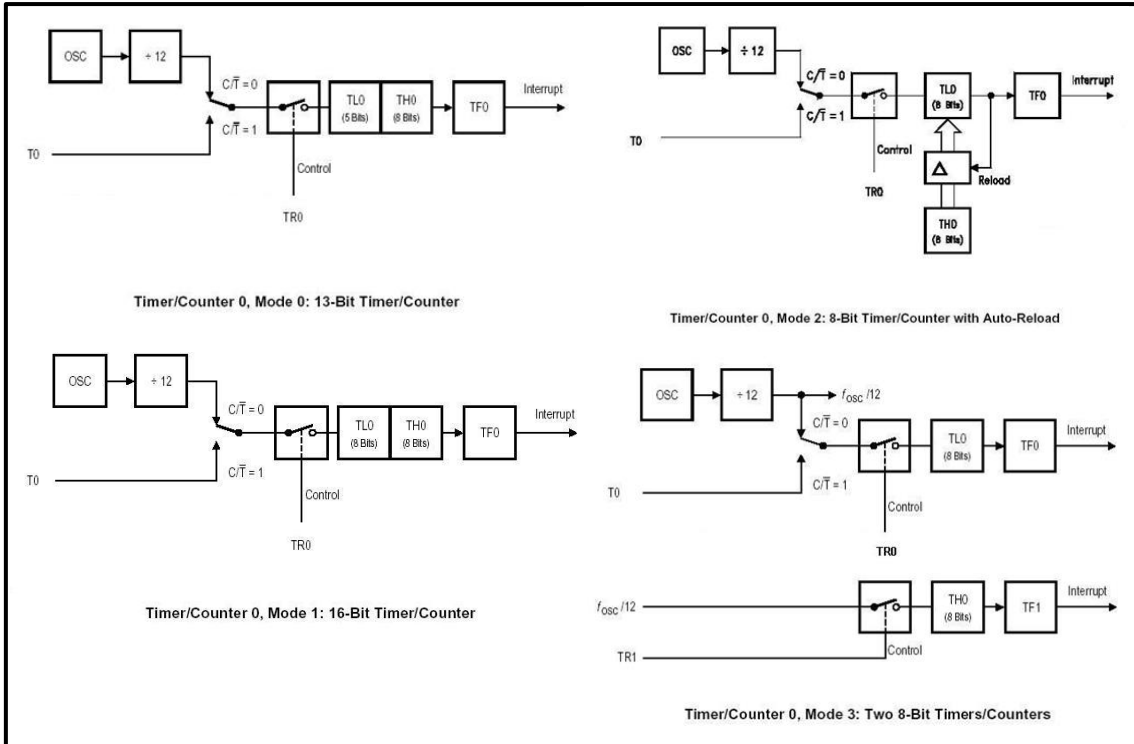
## 10 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.

- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



## 11 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 4 wires to minimize the number of added components and board area impact.

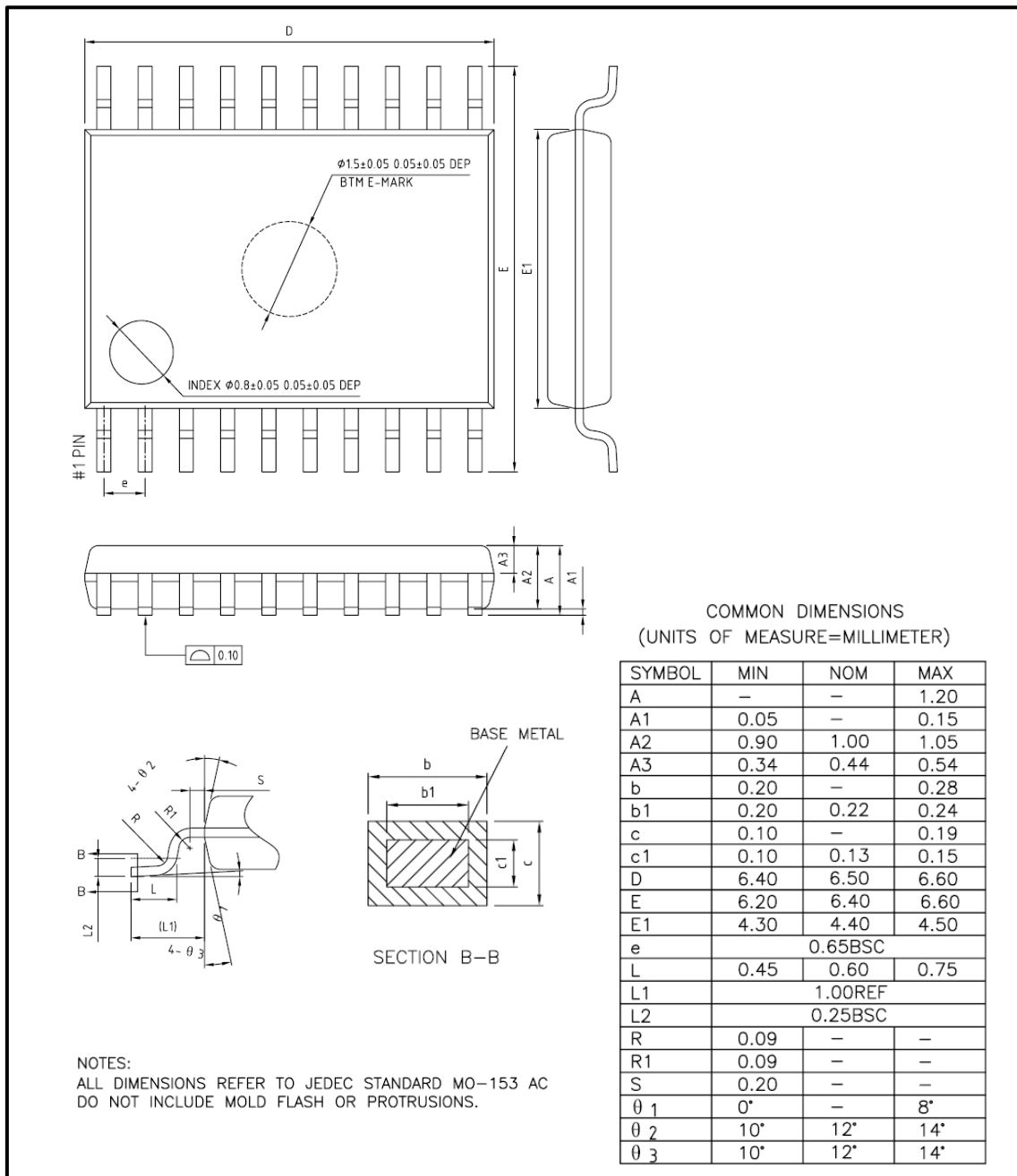
## 12 Ordering Information

Part No	Package	Program Flash	Data Flash	SRAM	I/O
DC6688F2STR	TSSOP20	2000B	16B	64B	18
DC6688F2STR-TR1	TSSOP20[1]	2000B	16B	64B	18
DC6688F2STM	TSSOP16	2000B	16B	64B	14
DC6688F2STM-TR1	TSSOP16[1]	2000B	16B	64B	14
DC6688F2STK	SOP16	2000B	16B	64B	14
DC6688F2STK-TR1	SOP16[1]	2000B	16B	64B	14

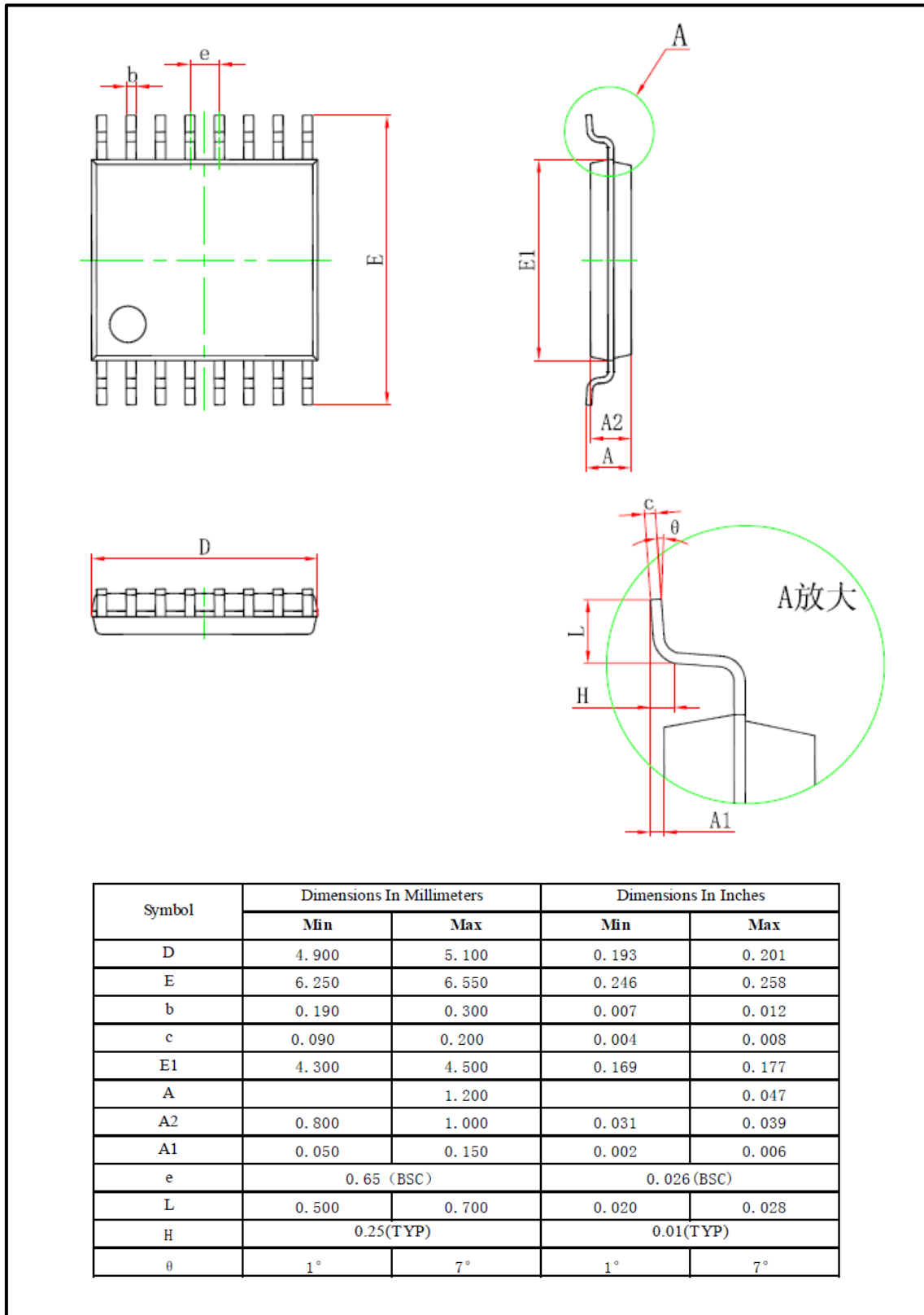
[1] Tape and reel packing.

## 13 Package Outlines

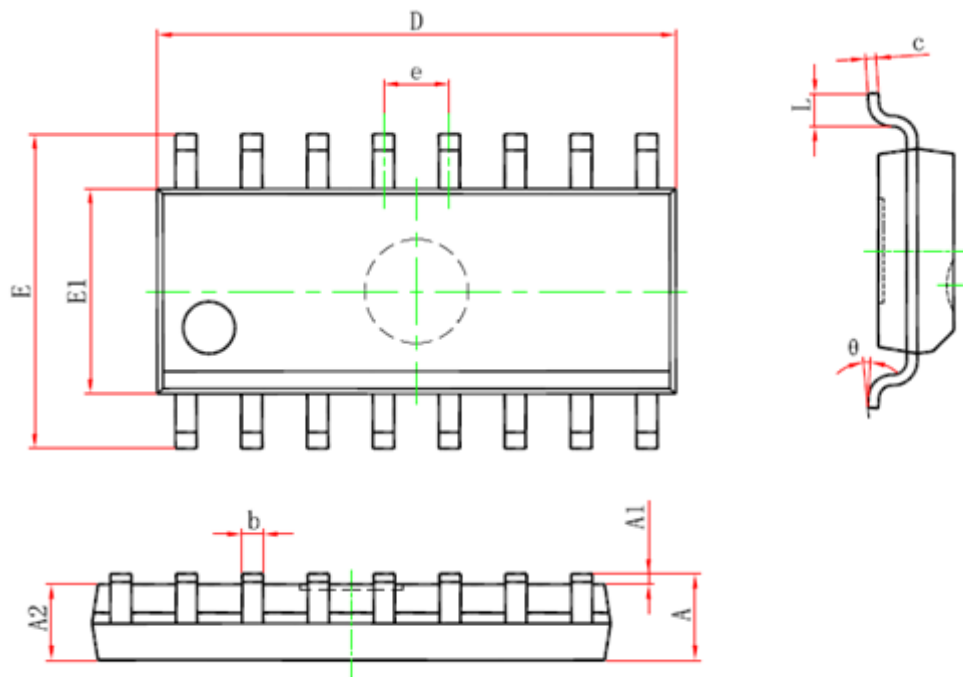
### 13.1 20-pin TSSOP



13.2 16-pin TSSOP



## 13.3 16-pin SOP



## NOTES:

ALL DIMENSIONS MEET JEDEC STANDARD MS-012 AC DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	---	1.750	---	0.069
A1	0.100	0.250	0.004	0.010
A2	1.400	1.500	0.055	0.059
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	9.800	10.200	0.386	0.402
e	1.270 (BSC)		0.050 (BSC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

## 14 Revision History

Document Rev No.	Issued Date	Section	Page	Description	Edited by	Reviewed by
1.0	6 Mar, 2014	All	-	New template	Kennis To	Celia Ki
1.1	5 Jun, 2014	2, 8, 12		Revised pin assignment. Added SOP16	Kennis To	Celia Ki
1.2	24 Jul, 2014	1		Revised run mode current and oscillator operating voltage	Kennis To	Fred Law
1.3	25 Jul, 2014	2		Removed PROG pin	Kennis To	Fred Law
1.4	21 Oct, 2014	12		Added DC6688F2STK-TR1	Kennis To	Philip Hung
1.5	19 Jan, 2014	1		Revised LVD and LVI spec	Kennis To	Philip Hung
1.6	10 Jan, 2017	1, 2		Revised LVI and 50kHz oscillator spec Add internal oscillator spec for IC factory programming option	Kennis To	Danny Ho
1.7	11 Jan, 2017	1		Corrected typo	Kennis To	Danny Ho
1.8	23 Nov, 2017	1		Revised LVI and internal oscillator spec	Kennis To	Danny Ho



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