DC6688FL32TC

Super 1T 8051 Microcontroller

DC6688FL32TC is an 8-bit Microcontroller Unit with low voltage embedded Flash memory, high accuracy system clock, high current drainage output, and IR receiving amplifier. It is manufactured in advanced CMOS process with Super 1T 8051 CPU core, Flash memory, and peripherals suitable for battery-operated & handheld device. As Flash memory is adopted in the MCU, firmware programming and upgrading (In System Programming) can be implemented which can significantly reduce development cycle time and dead inventory, as well as ability to perform in-application updates.

Features

- High-Performance 1T 8051 8-bit CPU core, MCS51 instructions compatible
- Idle, Power Down, and Backup modes
- Memory
  - 31.5KB Configurable Program & Data Flash Memory
  - Security bit for read back protection
  - Internal 256B SRAM; Expanded 1.5KB SRAM
- Internal 12MHz oscillator
  - ± 1% accuracy from -20°C to +70°C, V_{DD} = 1.8V
- Built-in transistor for IR LED (I_{OL} = 250mA at V_{OL} = 0.25V)
- IR generator by counter A with auto-reload function
- Built-in IR amplifier and a 24-bit Timer for learning module
- Code executes from Expanded SRAM
- 4-level priority interrupt controller
- 12 bit-programmable I/O ports
- Dedicated(TC version)/Muxed(TCC version) input pin for IR learning
- 16-bit Timers x 3
- 8-bit PWM Timer x 2
- Standard UART
- SPI Master
- I2C Master/Slave
- Low Voltage Detection (LVD) for backup mode
- Maximum operating voltage: 3.6V
- Operating temperature: -40°C to +85°C
- Package type:
  - 16-pin WLP

Quick look on Ordering Information

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1 Electrical Characteristics

1.1 Absolute Maximum Ratings

Parameter	Symbol	Conditions	Rating	Unit
Supply Voltage	V_{DD}	-	-0.3 to +3.8	V
Leads Input Voltage	V_{IN}	-	-0.3 to V_{DD} + 0.3	V
Operating Temperature	T_A	-	-40 to +85	°C
Storage Temperature	T_{STG}	-	-65 to +150	°C

1.2 DC Electrical Characteristics

(T_A = -40°C to +85°C, V_{DD} = 1.8 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}	f_{OSC} = 12MHz	V_{LVD1}	-	3.6	V
Input High Voltage	V_{IH1}	All input IO	0.7 V_{DD}	-	V_{DD}	V
Input Low Voltage	V_{IL1}	All input IO	0	-	0.3 V_{DD}	V
Output High Voltage	V_{OH}	All output IO I_{OH} = - 2mA, T_A = 25°C	V_{DD} - 0.5	-	-	V
Output Low Voltage[1]	V_{OL}	All output IO I_{OL} = 4.5mA, T_A = 25°C	-	0.4	0.5	V
PC1's IR Driver Current Sink	$I_{OL(IRDrv)}$	V_{OL} = 0.25V, IRDRV = 2, T_A = 25°C	-	250	-	mA
Input High Leakage Current	I_{LIH1}	All input IO except ISPSEL, V_{IN} = V_{DD}	-	-	1	µA
	I_{LIH3}	ISPSEL, V_{IN} = V_{DD}	-	-	100	µA
Input Low Leakage Current	I_{LIL1}	All input IO	-	-	-1	µA
Output High Leakage Current	I_{LOH}	All output IO, V_{OUT} = V_{DD}	-	-	1	µA
Output Low Leakage Current	I_{LOL}	All output IO, V_{OUT} = 0V	-	-	-1	µA
Pull-up Resistors	R_{PU}	V_{IN} = 0 V; T_A = 25°C	100	200	400	kΩ
Pull-down Resistors	R_{PD}	V_{IN} = 0 V; T_A = 25°C	100	200	400	kΩ
Run Mode Current[2]	Idd(op)	f_{OSC} = 12MHz, T_A = 25°C	-	2	5	mA
Power Down Current[3]	Idd(pd)	T_A = 25°C	-	1	2	µA

[1] The maximum total current $I_{OL(max)}$ and $I_{OL(min)}$, for all outputs combined, should not be exceed 40mA. This exclude the $I_{OL(IRDrv)}$ output.

[2] Supply current does not include current drawn through internal pull-up resistors or external output current loads, and is tested if the condition is that all ports configured to output push-pull.

[3] Supply current is tested if the condition is that:

a) Port A output open-drain.
b) Port B and C input enable pull-up resistor.
c) Port C1 output push-pull.
d) Port D output push-pull.
e) IR LED receiving signal amplifier is disabled

1.3 Low Voltage Detect Circuit

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Hysteresis Voltage of LVD (slew rate of LVD)	ΔV[1]		-	50	-	mV
Low Voltage Detect Level	V_{LVD1}		1.4	1.5	1.6	V

[1] V_{LVD2} - V_{LVD1} = ΔV

1.4 SRAM Data Retention

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention Voltage	V_{DDDR}		1.0	-	3.6	V
Data Retention Current	I_{DDDR}	V_{DDDR} = 1.0V	-	-	1	uA

1.5 Input/Output Capacitance

(T_A = -40°C to +85°C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Capacitance	C_{IN}	f = 1MHz; unmeasured pins are connected to V_{SS}	-	-	10	pF
Output Capacitance	C_{OUT}					
I/O Capacitance	C_{IO}					

1.6 Flash Memory Data Retention

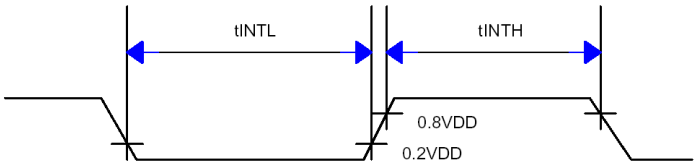
(V_{DD} = 1.8V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data Retention	t_{DRP1}	1 write/erase cycle	100	-	-	Year
	t_{DRP2}	10k write/erase cycle	10	-	-	Year
	t_{DRP3}	100k write/erase cycle	1	-	-	Year
Flash Write Voltage	V_{flash}	T_A = 25°C	1.5			V

1.7 Interrupt System

(T_A = -40°C to +85°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Setup Time for Rising/Falling Edge Interrupt Trigger	t_{INTH}, t_{INTL}	Port A, Port B, V_{DD} = 1.8V	1	-	-	cycle



Input Timing for Port A, B interrupts

1.8 System Clock

Parameter	Conditions	Min	Typ	Max	Unit
Internal 12MHz Oscillator	T_A = -20°C to +70°C V_{DD} = 1.8V ± 5%	-	-	±1%[1]	MHz
System Clock Frequency		f_{OSC}			
Stabilization Wait Time	Power up reset; LVD reset	-	$2^{19}/f_{OSC}$	-	ms
	External reset; Stop-mode wakeup	-	$2^{13}/f_{OSC}$	-	ms

[1] Design specification. Actual temperature range & variability may change based on silicon characterization

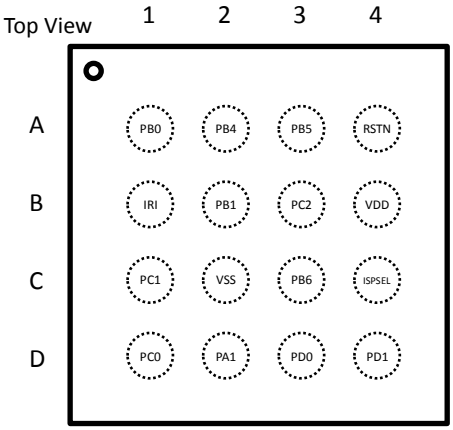
1.9 Infrared Learning Module

(V_{DD} = 1.8V, T_A = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
IRI Amplifier Input Low Detection	IRI_{DL}	V_{DD} = 1.8V	-	-	0.22	uA
IRI Amplifier Input High Detection	IRI_{DH}	V_{DD} = 1.8V	1.27	-	-	uA

2 Pin Assignment

WLP 16



WLP 16	Pin Name	Fucntion								
		Inter-rupt	IR Tx/Rx	PWM	Timer 0,1,2	Timer 24	UART	I^2C	SPI	ISP
A1	PB0	INTB					RXD0		SDI	SCK
B2	PB1	INTB					TXD0		SDO	MOSI
A2	PB4	INTB						SCL1	SCK	
A3	PB5	INTB		PWM0				SDA1		
C3	PB6	INTB		PWM1	T2EX	T24EX				ECLK2
B3	PC2	INTC			T2	T24CLK				
C1[1]	PC1	INTC	IR Tx		T1					
D1	PC0	INTC			T0					SS
D2	PA1	INTA								MISO
B1[1]	IRI		IR Rx							
D3	PD0									SL
D4	PD1									ECLK
C4	ISPSEL									ISPSEL
B4	VDD									VDD
C2	VSS									VSS
A4	RSTN									

[1] IRI & PC1 are bonded together on TCC package

3 Description

DC6688FL32TC is a Super 1T CPU cored Microcontroller Unit designed for low-power applications on battery-operated handheld device where PCB area is at a premium. The DC6688FL32TC incorporates a high performance 8-bit 8051 CPU with low voltage embedded Flash memory, built-in high accuracy oscillator, high current drainage output, IR LED diode receiving signal amplifier, and other peripherals such as USART, SPI, I^2C.

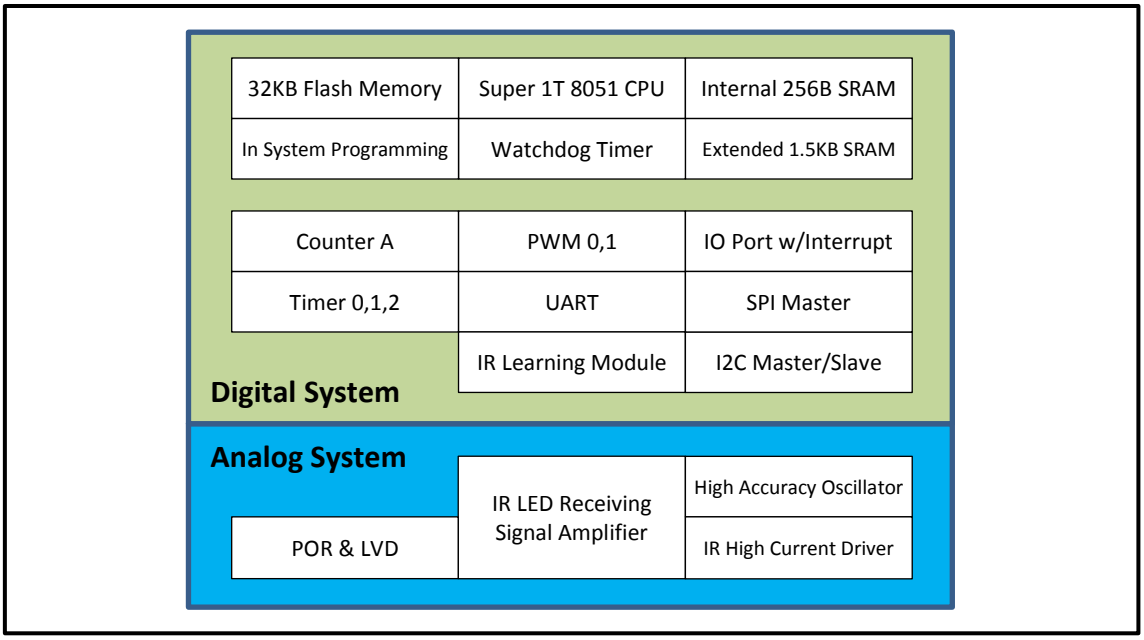
The Super 1T CPU core incorporate in DC6688FL32TC is a high performance 8051 8-bit CPU with instruction execution time as low as 125ns on a 8Mhz operating clock. With performance upto 12 times faster than the original 8051 CPU, this core allows applications to use slow system clock for better power consumption, an important attributes to all battery-operated products.

The DC6688FL32TC embedded Flash memory allows firmware programming and upgrading via In System Programming (ISP) which can significantly reduce development cycle time and dead inventory. Multiple firmware can be made to use the same MCU without worry problems of long mask ROM cycle time, inventory burden, end customers rescheduling. ISP can be implemented into the target application easily where firmware change can be incorporated into PCB assembly process, or even after production assemble on final product.

The Flash memory can be partitioned to Program and Data area in 512 Byte increment to suit any application. The Data Flash memory can be used to store user data and the function is just same as EEPROM. The DC6688FL32TC is also able to update and Flash memory by firmware itself, with protection area and signature guarding accidental access, enabling application to update the firmware in the field.

The DC6688FL32TC's highly accurate clock generator for used as the MCU's system clock can generate 12/8/6/4/2/1MHz without any external components. The clock generator also supports additional trimming and verification by In-System Programmer to ensure the clock accuracy.

DC6688FL32TC has a dedicated carrier frequency generator (Counter A), a modulation mux, and a high current drainage output for one chip IR remote controller application. The chip also has an IR LED receiving signal amplifier and a specialized 24 bit timer to facilitate external circuit free IR learning function.



DC6688FL32TC System Block Diagram

4 Memory

Memory comprises of the following elements, namely:

- 31.5KB Program Flash memory + Data Flash memory
- 256B Internal SRAM
- 1.5KB Expanded SRAM
- 128B Special function register (SFR)
- 256B External special function register (XFR)

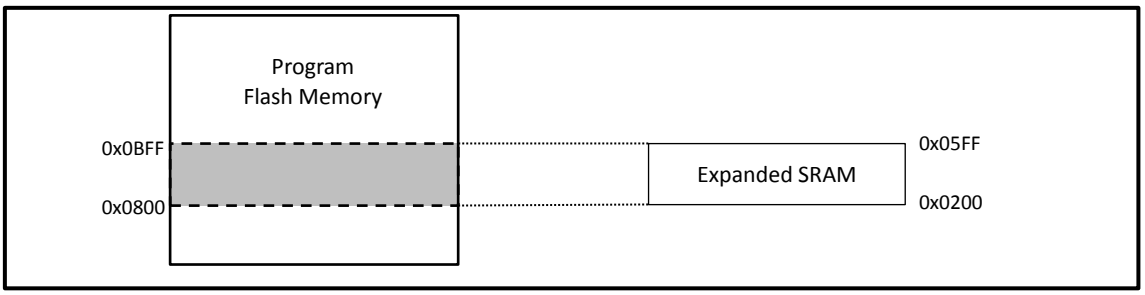
4.1 Program & Data Flash Memory

On-chip program Flash size is configurable, range from 2.5kilobytes to 31.5kilobytes, upon different application. It can be programmed by In-System-Programming (ISP) method where firmware can be updated during PCB assembly.

In addition, the program and data Flash memory can be updated by firmware itself, hence enable firmware to be updated on the field. Write protection area as well as write enable signature are available to avoid writing accidentally.

4.2 Code Executable from SRAM

Code execution enables the mapping of expanded SRAM to the program code memory and allows code to be run on the SRAM location.



4.3 Special Function Register (SFR)

All memory mapped SFRs, except the program counter and the four 8-register banks, resides in the special function register address space. These registers include arithmetic registers, pointers, I/O-ports, registers for the interrupt system, timers, watchdog timer, UART, etc. Some locations in the SFR address space are addressable as bits.

4.4 External Function Register (XFR)

The external function register (XFR) is 256-byte memory area that is logically located in the built-in memory space. This is accessed like external RAM (MOVX instructions). This area is reserved for controlling and accessing the on-chip peripherals additional to standard 8051 core.

5 Central Processing Unit (CPU)

The 1T 8051 CPU (Central Processing Unit) is MCS51 instruction compatible. It consists of the instruction decoder, the arithmetic section and the program control section. Each program instruction is decoded by the instruction decoder. This unit generates the internal signals controlling the functions of the individual units within the CPU. They have an effect on the source and destination of data transfers and control the ALU processing.

The arithmetic section of the processor performs extensive data manipulation and is comprised of the arithmetic/logic unit (ALU), A register, B register and PSW register. The ALU accepts 8-bit data words from one or two sources and generates an 8-bit result under the control of the instruction decoder. The ALU performs the arithmetic operations add, subtract, multiply, divide, increment, decrement, BDC-decimal-add-adjust and compare, and the logic operations AND, OR, Exclusive OR, complement and rotate (right, left or swap nibble (left four)). Also included is a Boolean processor performing the bit operations as set, clear, complement, jump-if-not-set, jump-if-set-and-clear and move to/from carry. Between any addressable bit (and its complement) and the carry flag, it can perform the bit operations of logical AND or logical OR with the result returned to the carry flag.

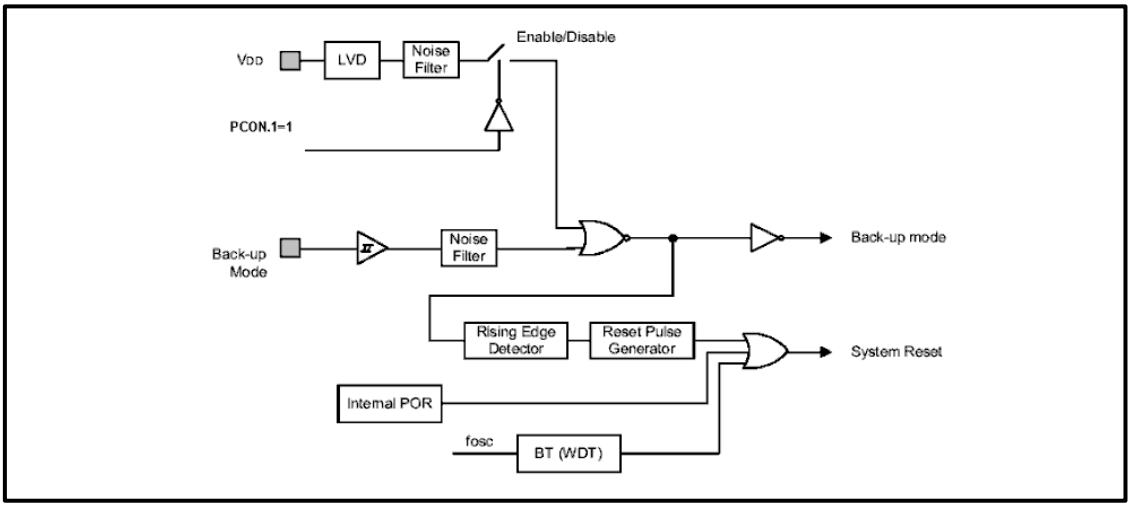
The program control section controls the sequence in which the instructions stored in program memory are executed. The 16-bit program counter (PC) holds the address of the next instruction to be executed. The conditional branch logic enables internal and external events to the processor to cause a change in the program execution sequence.

6 Low Voltage Detection Reset

The on-chip Low Voltage Detect circuit generates a system reset. It detects the level of V_{DD} by comparing the voltage at pin V_{DD} with reference voltage, V_{LVD1} (Low Voltage Detect Voltage Level 1). Whenever the voltage at V_{DD} is falling down and passing V_{LVD1}, the IC goes into back-up mode at the moment "V_{DD} = V_{LVD1}".

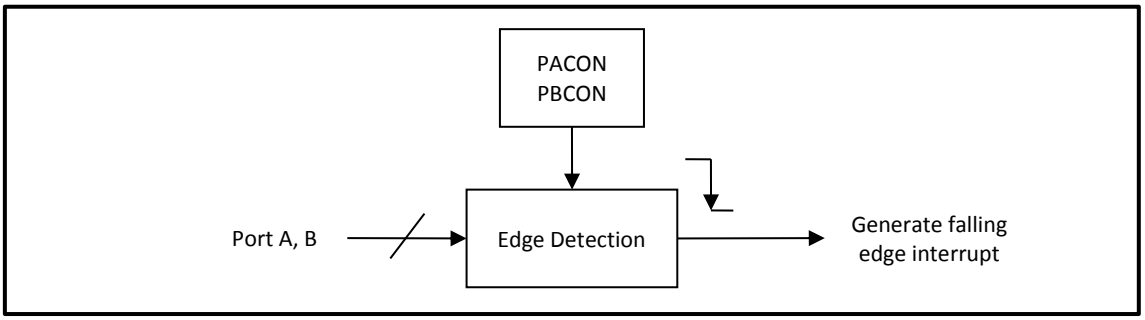
On the other hand, system reset pulse is generated by the rising slope of V_{DD}. While the voltage at pin V_{DD} is rising up and passing V_{LVD2} (Low Voltage Detect Voltage Level 2), the reset pulse is occurred at the moment "V_{DD} >= V_{LVD2}".

LVD provides a hysteresis (V_{LVD2} –V_{LVD1}) to avoid the oscillation near the decision level. For the sake of reducing the current consumption, this function can be disabled when the IC is in power down mode.



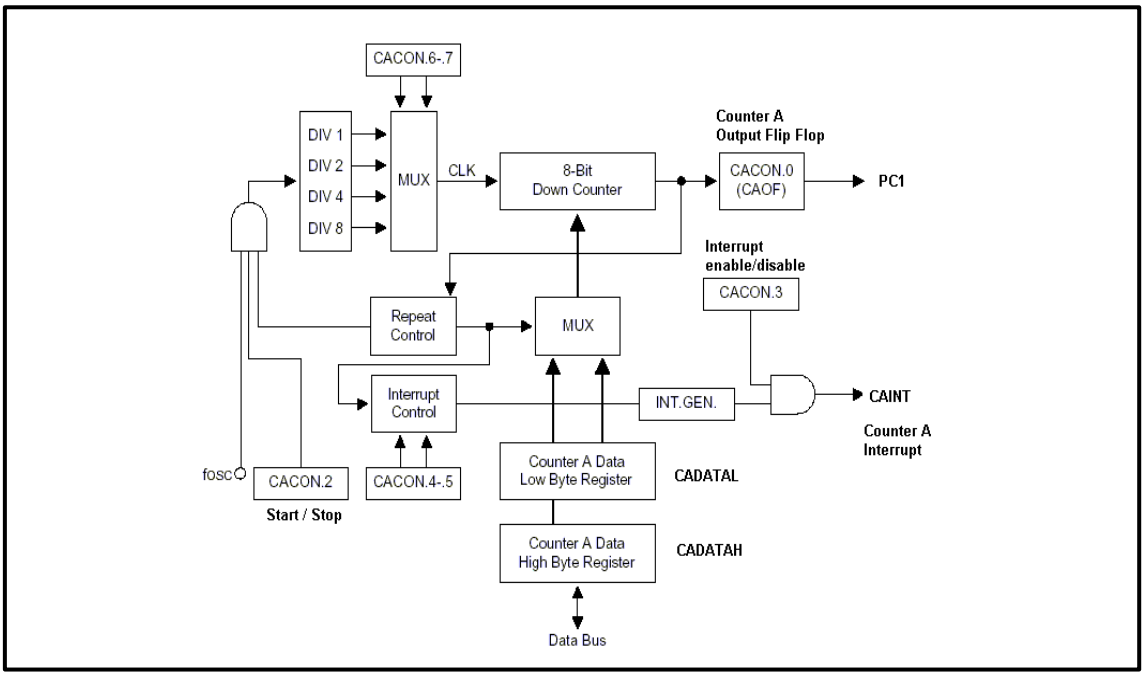
7 I/O port

For FL32TC, the 16-pin WLP package has one 1-bit port (PA), one 5-bit port (PB), one 3-bit port (PORTC) and one 2-bit port (PORTD). All ports are latches used to drive the bi-directional I/O lines. On reset, Port A and Port B are set to the value (XXXXXXXX). Port C is set to the value (XXXXXXXX). Port D is set the value (00011111).



8 Counter A (IR Carrier Frequency Generator)

Counter A is a PWM module that can generate waveform with f_osc clock. It can be used to generate the carrier frequency of remote controller. It has also a 16-bit count down counter with auto reload function for automatic IR coding modulation.

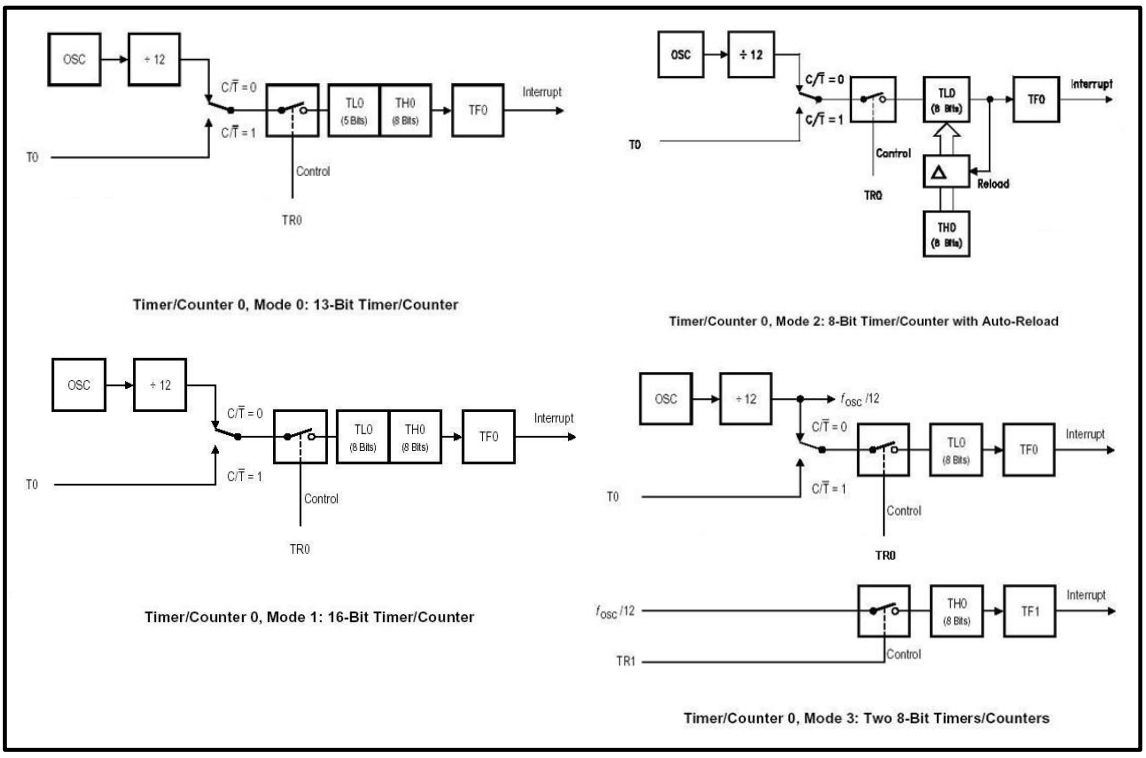


9 General Purpose Timers/Counters

Three independent general purpose 16-bit timers/counters, Timer0, Timer1 and Timer2 are integrated for use in counting events, and causing periodic (repetitive) interrupts. Either can be configured to operate as timer or event counter. In the 'timer' function, the registers TLx and/or THx (x = 0, 1) are incremented once every machine cycle. Thus, one can think of it as counting machine cycles.

Regarding the 'counter' function, the registers TLx and/or THx (x = 0, 1) are incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled during every machine cycle. When the samples show a high in one cycle and a low in the next cycle, the count is incremented. The new count value appears in the register during the cycle following the one in which the transition was detected. Since it takes 2 machine cycles (24 oscillator periods) to recognize a 1-to-0 transition, the maximum count rate is 1/24 of the oscillator frequency. There are no restrictions on the duty cycle of the external input signal, but to ensure that a given level is sampled at least once before it changes, it should be held for at least one full machine cycle.

Timer 2 has several features on top of Timer 0 and 1. It runs in 16-bit mode.
- 16-bit timer/counter
- 16-bit timer with capture
- 16-bit auto-reload timer/counter with up/down count
- Timer output generator



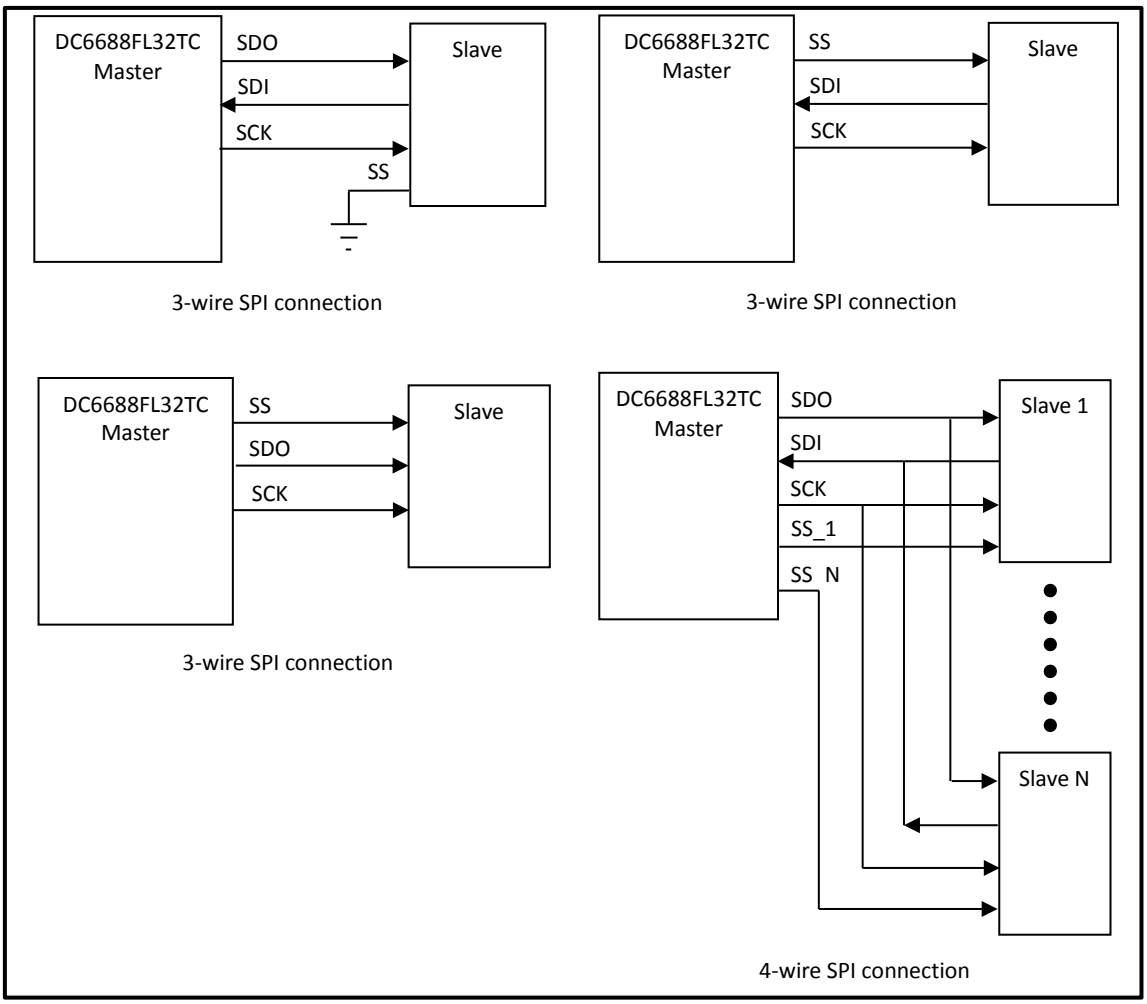
10 Enhanced UART

The Enhanced UART interface is fully compatible with the standard 8051 serial channel, and can operates in one of four modes (one synchronous and three asynchronous). It is a 2 wire interface that supports full duplex communication in asynchronous mode and half duplex communication in synchronous mode. The baud rate can be generated by timers or the hardware fractional clock divider for high timing accuracy communication. A 9 bit communication mode is included for parity or multi-device bus support that filters communication without CPU processing.

Mode	Type	Description
0	Synchronous (Half Duplex)	Baud rate: f_osc/12, 8-bit communication
1	Asynchronous (Full Duplex)	Baud rate: Variable, 8-bit communication
2	Asynchronous (Full Duplex)	Baud rate: f_osc/64 or 32, 9-bit communication
3	Asynchronous (Full Duplex)	Baud rate: Variable, 9-bit communication

11 Serial Peripheral Interface

The integrated Serial Peripheral Interface (SPI) master allows eight bits of data to be synchronously transmitted and received simultaneously at rate up to 3MHz.
The hardware connection methods are shown below.



12 Inter-Integrated Circuit (I2C) Interface

The I2C Bus Controller supports all transfer modes from and to the I2C bus. The I2C bus uses two wires to transfer information between devices connected to the bus: “SCL” (serial clock line) and “SDA” (serial data line). The I2C Interface handles byte transfer autonomously and keeps track of serial transfers.

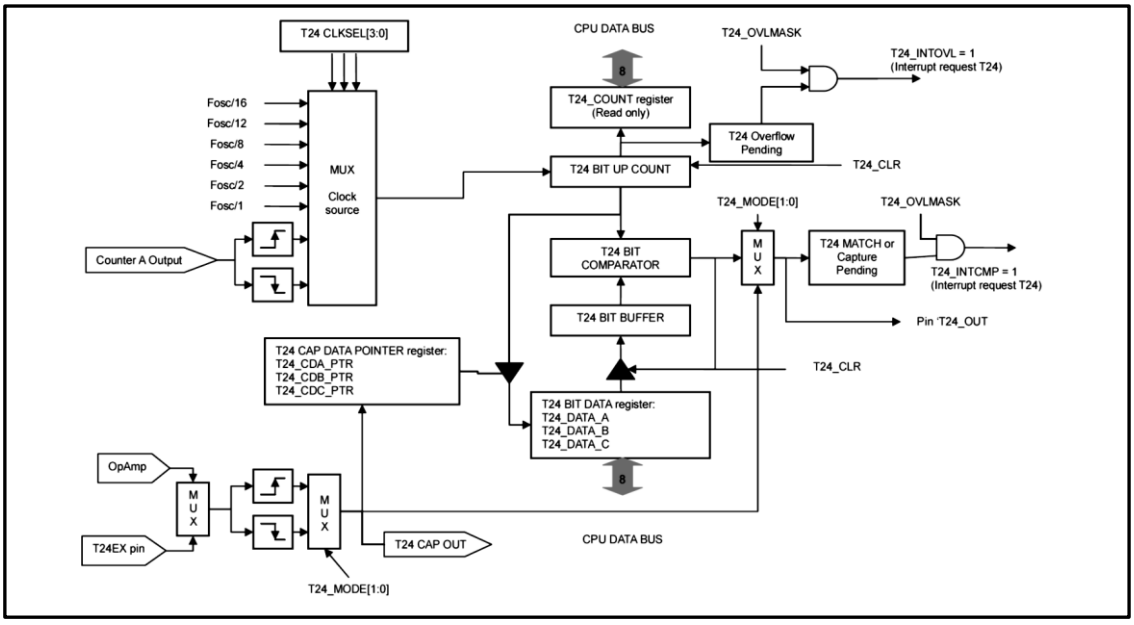
The I2C component performs 8-bit-oriented, bi-directional data transfers up to 100 Kbit/s in the standard mode or up to 400 Kbit/s in the fast mode in master or slave mode.

Mode	Description
Master Mode	Initiate data transmit & receive via START and STOP signals on SDA, while driving SCL for signal clock
Slave Mode	Responds to START and STOP signal for data receive & transmit via SDA, while using driven SCL as signal clock

13 Infrared Learning Module

IR learning module includes IR receiver and T24 timer. With the built-in Op Amp circuit, no external amplifier circuit is needed. Analog signal entering IRI pin is converted to digital signal by IR receiver, and feed to T24 timer.

The high resolution 24-bit timer provides a high capability of IR learning. It can capture carrier frequency as high as 500kHz.



14 In System Programming

The In System Programming (ISP) feature allows the update of Flash program memory content when the chip is already plugged on the application board. It requires 6 wires to minimize the number of added components and board area impact

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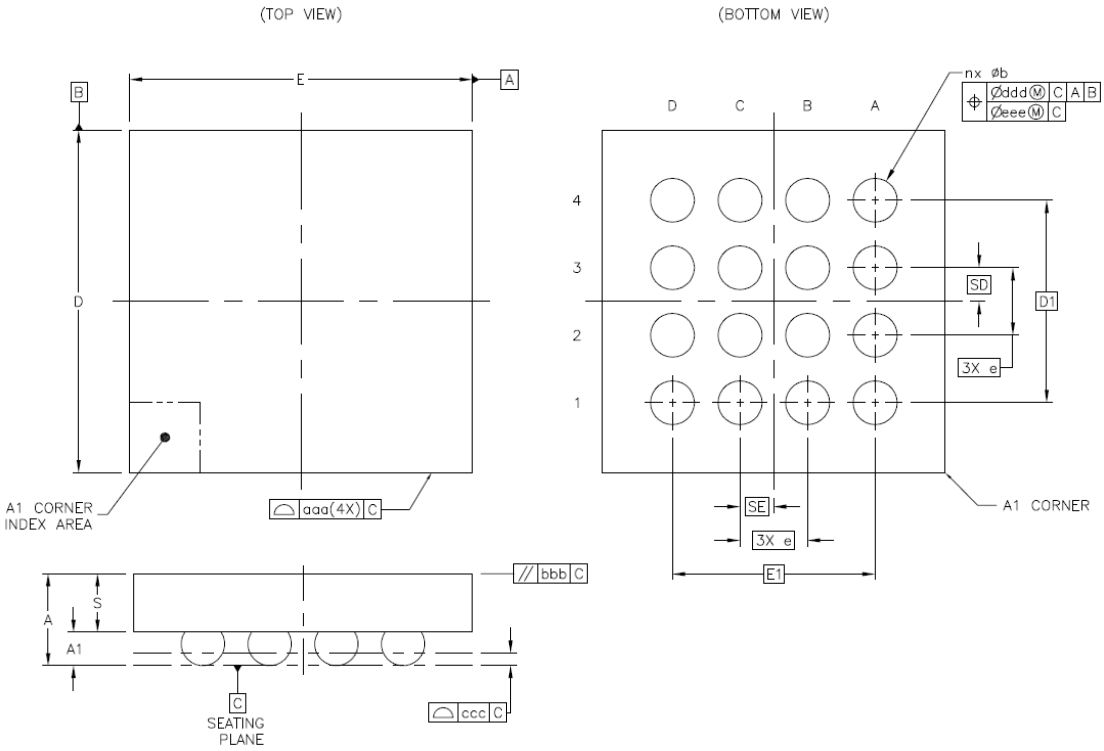
15 Ordering Information

Part No	Package	Program & Data Flash	SRAM	I/O	IR Receiving Lead
DC6688FL32TC	WLP16	31.5KB	256B + 1.5KB	12	Dedicated
DC6688FL32TCC	WLP16	31.5KB	256B + 1.5KB	12	Joined with PC1

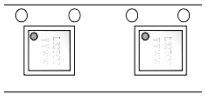
16 Package Outlines

16.1 16-pin WLP



		SYMBOL	COMMON DIMENSIONS
TOTAL THICKNESS		A	0.59 ± 0.059
WAFER THICKNESS		S	0.35 ± 0.025
STAND OFF		A1	0.17 ~ 0.23
FILM THICKNESS		A2	0.04 ± 0.004
BODY SIZE	X	E	1.89
	Y	D	1.89
BALL/BUMP PITCH	X	SE	0.2 BSC
	Y	SD	0.2 BSC
EDGE BALL CENTER TO CENTER	X	E1	1.2 BSC
	Y	D1	1.2 BSC
PITCH		e	0.4 BSC
BALL DIAMETER (SIZE)			0.25
BALL/BUMP WIDTH		b	0.23 ~ 0.29
BALL/BUMP COUNT		n	16
PACKAGE EDGE TOLERANCE		aaa	0.03
WAFER FLATNESS		bbb	0.06
COPLANARITY		ccc	0.05
BALL/BUMP OFFSET (PACKAGE)		ddd	0.015

TAPE & REEL DIE DIRECTION



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